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Comparative Analysis of CMOS and SOI CMOS Analog-Digital Switches For SoC Under Extreme Conditions

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The paper investigates the design and performance of integrated analog-digital switches (ADS) targeted for sensor micro-systems-on-a-chip (MSoC). As modern sensor systems require high accuracy and energy efficiency, the choice of appropriate semiconductor technology becomes highly critical. Modern sensor micro-systems-on-a-chip (MSoC) require high-precision and energy-efficient analog-digital switches (ADS) capable of operating under extreme environmental conditions.

Computer simulations were conducted using 120 nm design rules, accounting for parasitic layout effects, charge injection, and substrate influence. Identical physical layouts for both bulk CMOS and SOI CMOS versions of the devices were developed to ensure a consistent and valid comparison.

The simulation results demonstrate that SOI CMOS switches provide significantly higher linearity and lower leakage currents (in the picoampere range versus nanoamperes). It was established that the power consumption of the SOI-based switch is, on average, 4.5 times lower than its bulk CMOS counterpart across the temperature range from –50 °C to +200 °C. Furthermore, while the bulk CMOS switch fails at temperatures exceeding 175 °C, the SOI CMOS device maintains full functionality up to 200 °C. The results confirm that SOI CMOS structures are the optimal choice for MSoC operating in extreme environments. The proposed three-output switch design effectively converts sinusoidal signals into pulses, making it suitable for biomedical sensors and charge-transfer circuits.

Keywords: SOI CMOS technology, analog-digital switch, micro-system-on-chip (MSoC), charge injection, power consumption, high-temperature electronics, 120 nm process.

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Introduction

In modern sensor microsystems-on-a-chip (SOC), analog switches are critical elements for switching weak signals from primary converters to processing circuits, e.g., (analog-to-digital converters (ADCs), operational amplifiers (OPs), amplifiers, etc.). Analog-to-digital switches (ADSs) usually do not contain sensor elements, but contain traditional CMOS transistor structures, therefore, standard bulk CMOS technology of integrated circuits (ICs) is used for their manufacture, however, the operation of the SoC requires increased accuracy, meeting the requirements of extreme operating conditions and improving the energy efficiency of the sensor SoC as a whole. Therefore, a more promising technology for this purpose may be SOI (silicon-on-insulator) CMOS transistor structures[1,2,4]. The presence of several levels of output signals in the SoC for controlling interface outputs is important. For their formation, additional elements can be introduced into the ADS, e.g., inverter amplifiers with separate power sources, which will ensure the switching of weak analog signals into pulses of different polarity with different signal levels. Therefore, the work is devoted to the comparative analysis and computer modeling of the ADS with CMOS and SOI CMOS structures for microsystem applications.

Objective. The aim of this work is to provide a comparative analysis and computer simulation of ADS based on standard bulk 120 nm CMOS and Silicon-on-Insulator (SOI) CMOS technologies, with a specific focus on their performance under high-temperature stress.

I. Features of CMOS and SOI CMOS integrated switches

Traditional CMOS structures are based on a pair of complementary n- and p-channel MOS transistors. Their advantages are standard, industrial (bulk) CMOS technology of integrated circuits (ICs), which integrates well with digital control circuits on a single IC or sensor SoC. Disadvantages for sensor microsystems are the presence of a body effect, which manifests itself in the influence of a change in threshold voltage when the drain potential changes on the nonlinearity of the resistance of the open channel of the MOS transistor. In addition, parasitic loss currents arise through the p-n junctions of the MOS transistors, parasitic "latching" effects of CMOS transistors, which is critical for precision sensor SoCs.

Silicon-on-insulator (SOI) technology of CMOS structures involves the formation of CMOS transistors on a thin layer of insulator, usually made of silicon oxide SiO_2, separated from a silicon substrate. Such structures are significantly more stable under extreme operating conditions, radiation and high temperatures, which is important for extreme and special operating conditions [9,11]. In SOI CMOS elements, due to dielectric insulation and, as a result, minimal parasitic capacitances of p-n junctions, the possibility of switching high-frequency signals without distortion is significantly increased [13].

In the SOI of the CMOS elements, there is no "latching" effect, which is associated with the dielectric insulation of the elements, which prevents the formation of parasitic thyristor structures, and the resistance of the open SOI of the MOS transistor is significantly more stable in a wide range of input voltages.

The physical processes in analog-to-digital switches determine the accuracy of the signal transmission from the sensor. When a transistor transitions from the "on" state to the "off" state, two main parasitic effects occur: charge injection and clock signal propagation.

Charge injection is the most critical process for sensor SoC. When a voltage is applied to the gate to close the channel, the mobile charge carriers (electrons in the n-channel or holes in the p-channel) that formed this channel must somehow be absorbed. A feature of the charge injection mechanism in CMOS structures is that the charge is distributed between the drain and source, and part of the charge enters the analog line, which causes a jump (pulse release) on the load capacitance. In bulk CMOS structures, this effect is compensated by a complementary pair (n- and p-channels simultaneously) for mutual annihilation of charge carriers, however, due to the different mobility of electrons and holes, complete compensation is impossible. For SOI CMOS structures, due to the thin active silicon-on-insulator layer, the volume of the transistor body is significantly smaller compared to CMOS, which in turn reduces the number of charge carriers in the channel and limits their outflow paths, which is an advantage of SOI CMOS structures and significantly reduces the error from charge injection.

Features of the passage of the clock signal. This process is due to parasitic capacitances between the gate and the source, and the gate and the drain. For bulk CMOS transistors, the gate and channel are separated by a sub-gate dielectric and form a capacitor. The voltage jump on the gate through this capacitor can be directly transmitted to the analog circuit, which leads to the appearance of a short-term noise [3,5].

In SOI CMOS structures, there is no “channel-substrate” capacitance, and the geometric dimensions of the junctions are significantly smaller, since the junctions are formed by the vertical walls of the SOI layer, and a capacitance is connected in series to the “channel-substrate” capacitance through an insulating thick oxide to the main substrate. In total, this allows you to significantly reduce the total parasitic capacitance, making the “passage” of the clock signal minimal.

The influence of the body effect and linearity. In CMOS transistors, the substrate potential affects the threshold voltage. During the passage of a signal of variable amplitude, it constantly “floats”, which modulates the channel resistance and creates harmonic distortions. In SOI CMOS transistors, they can have a “floating” substrate or an individual connection of the contact to the body of the subchannel region. This allows stabilization relative to the source, ensuring ideal linearity of signal transmission from the sensor. Therefore, although bulk CMOS technology remains economically advantageous for consumer electronics, SOI CMOS technology is an unalternative choice for high-precision sensor SoCs. It provides a minimum level of noise, the absence of mutual interference between channels and stable operation in difficult operating conditions [6,7].

II. Circuit Design and Layout of the Integrated Multilevel Analog-Digital Commutator

To implement an integrated element of an ADS, inverter CMOS and TOF CMOS elements and a through-hole two-way switch were used. The electrical schematic diagram of an ADS for an integrated version is shown in Figure 1.

In the circuit according to Fig. 1 – V1 – the source of the pulse signal of the Enable permission, which is fed to the input of the inverter (transistors n-channel M1 and p-channel M2) and the gate of the transistor M3, and the inverted signal of the n-Enable permission from the output

Table 1.

Basic comparative analysis for sensory MoCs

Characteristics	Bulk CMOS structures	SOI CMOS structures
Channel isolation	Medium (due to p-, n-junctions in the substrate)	High (dielectric)
Leakage current	Nanoamperes	Picoamperes
Linearity	Depends on voltage	High stability
Density	High	Very high

of the inverter – controls the p-channel transistor M4. Transistors M3 and M4 are connected in parallel and form a two-way pass-through key. The signal is fed to the n-channel MOS transistor M3 from the source side, and to the p-channel M4 - from the drain. Such inclusion ensures good transmission of both high and low signal levels to the output of the pass-through key OUT DATA.

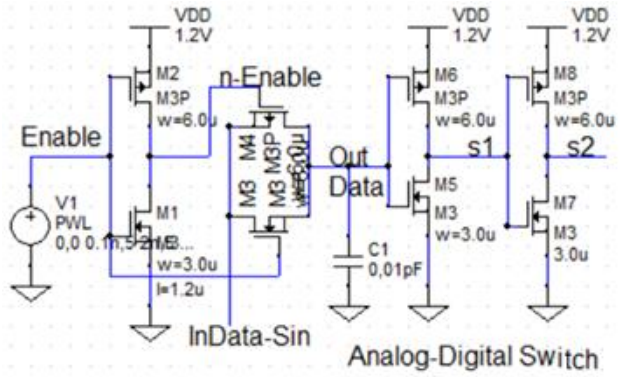

Fig. 1. Electrical schematic diagram of a three-output analog-digital switch (V1 – Enable signal; InData-Sin – input analog signal; C1 – virtual capacitance.

The switching signal is formed on a virtual capacitance C1=0.01 pF, at an interval of 3 amplitudes of the input sinusoidal signal InDataSin, which will be translated into a pulsed switching signal in time with the enable signal. This switching signal is fed to two series-connected inverter-amplifiers (transistors M5-M6 and M7-M8, respectively), from the outputs of which we receive direct and inverted signals. All inverters are powered by a supply voltage of Vdd = 1.2 V, which corresponds to the specified length of the transistor channels. In the case of the need to form several levels of ADS signals, e.g., to control external interfaces, the supply voltages of the output inverters can be increased in accordance with the proportionally increased lengths and widths of the channels of transistors M5-M6, and - or M7-M8, e.g., up to 2.4V.

Thus, at the output of the switch we get three control signals - DATA OUT, s11 and inverse s12. The value of the virtual capacitance C1 affects the process of converting a sinusoidal signal into a pulsed one, but for example, already at values of C1=0.05 pF and more - the sinusoid within the duration of the permission signal is significantly distorted. This feature can be used to build sensitive pico-capacitive sensor elements, for example, when connecting integrated pico-capacitors in series, which will respond to the short circuit of one or more series-connected ones.

CMOS and SOI CMOS topologies of the ACS according to the scheme in Fig. 1 are shown in Fig. 2. The features of CMOS and SOI CMOS topologies are that in

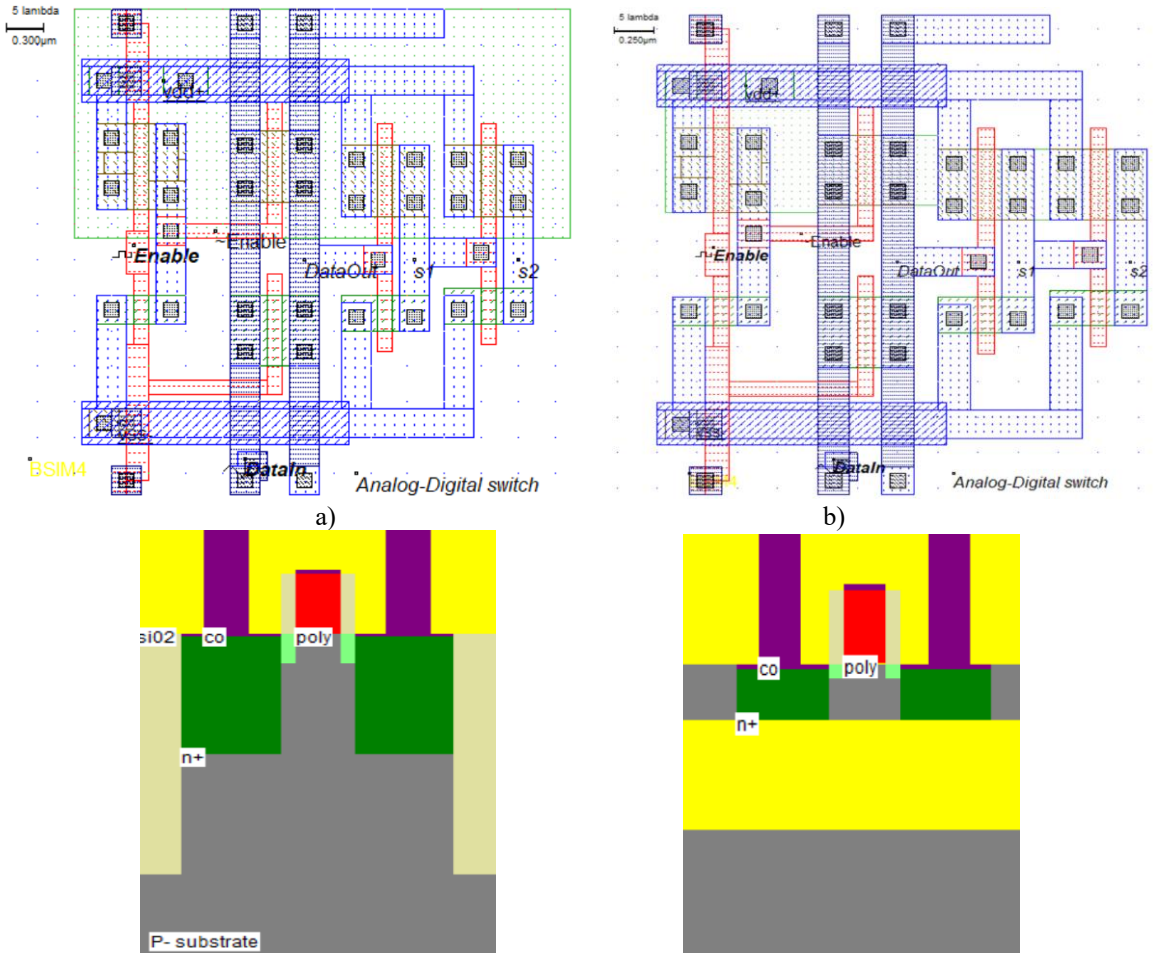

Fig. 2. Comparison of ACS topologies in the 120 nm process: (a) on standard CMOS structures; (b) on SOI CMOS structures; (c) cross-section of a bulk-channel MOS transistor; (d) cross-section of an n-channel MOS transistor on an insulator (SiO_2).

order to compare the simulation results, they are designed to be virtually identical in terms of the geometric dimensions of the transistors, their location and configurations.

In the SOI CMOS variant, similar to CMOS, an analogue of n-type conductivity pockets for the SOI film and the application of a bias voltage from the supply voltage Vdd to them is technologically introduced, which ensures optimal functioning of p-channel SOI MOS transistors of the ACS. N-channel MOS transistors are implemented directly in an undoped SOI film on an insulator. To compare the results of the temperature effect, the location and dimensions of the pockets are similar compared to CMOS and are maximally identical. However, optimization of this parameter would allow significantly reducing the area of the topology in the SOI CMOS variant [8,13].

The layouts are made according to the design and technological standards of the 0.12 µm (120 nm) technology, the lengths of the transistor channels are 0.12 µm, the widths of the n-channel transistor channels are 0.30 µm, and the widths of the p-channel transistor channels are 0.6 µm. This ratio of dimensions ensures symmetry of the currents of both types of transistors. The results of computer simulation of the ADS are presented in Fig. 3, and a comparative analysis of power consumption is presented in Table 2 and Fig. 4.

As can be seen from the table of simulation results and the power consumption graph in the temperature range from minus 50 °C to 200 °C with a step of 25 °C, the power consumption varies for the CMOS element from 10.74 µW to 42.76 µW, and there is a distortion of the shape of the output signals at temperatures above 175 °C. For the SOI CMOS element, the power consumption during simulation under the same conditions varies from 2.54 µW (-50 °C) to 8.47 µW (200 °C). Specifically, the power consumption of the multilevel analog-digital commutator based on SOI CMOS structures is, on average, 4.2 times lower than that of its bulk CMOS counterpart at low temperatures, and 5.05 times lower at high temperatures (200 °C).

Due to the minimal leakage currents, minimal parasitic capacitances, and temperature stability [14], analog to digital commutator and SOI can be used in sensor SoC, including those with three-dimensional elements [16], as switches in charge transfer circuits, in image matrices, biomedical sensors [16], and in studies of signals with amplitudes in millivolts.

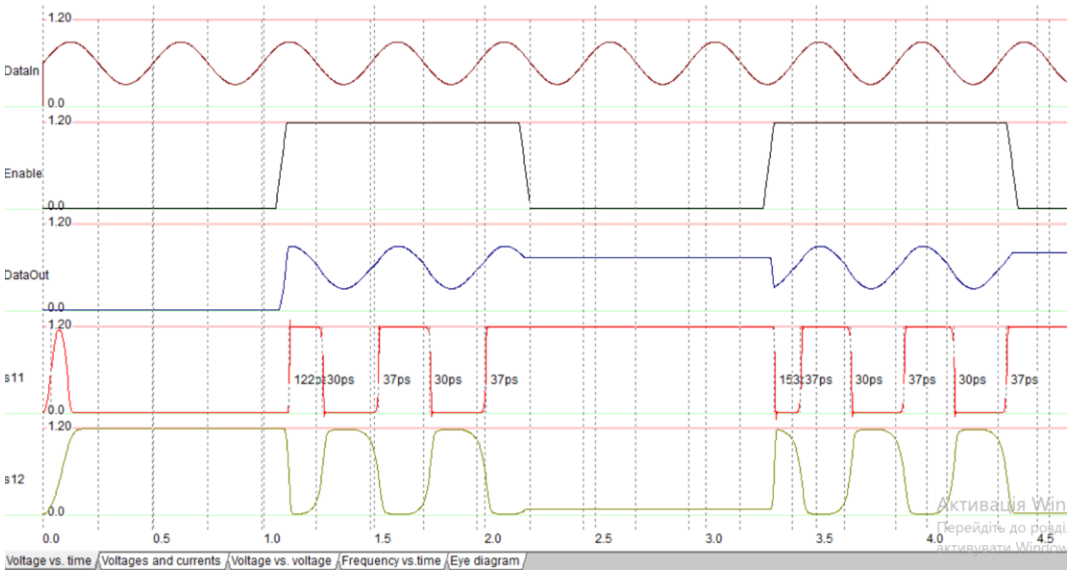

Fig. 3. Oscillograms of the simulation of the integral SOI of the CMOS switch directly from the layouts (according to Fig. 2, top to bottom): time dependences of the input sinusoidal signal (InData-Sin), the enable signal (Enable) and the output pulse signals (DataOut, s11, s12).

Table 2.

Comparative simulation results of power consumption versus temperature for bulk CMOS and SOI CMOS integrated ADCs (Commutators).

T, °C	-50	-25	0	25	50	75	100	125	150	175	200
P, µW Bulk CMOS	10.74	13.33	16.27	19.41	22.55	25.58	28.47	31.31	34.33	37.98	42.76
Stable Operating Temperature Range	+	+	+	+	+	+	+	+	+	Output waveform distortion	Output waveform distortion
P, µW SOI CMOS	2.54	2.85	3.25	3.74	4.31	4.49	5.61	6.31	7.02	7.74	8.47
Stable Operating Temperature Range	+	+	+	+	+	+	+	+	+	+	+

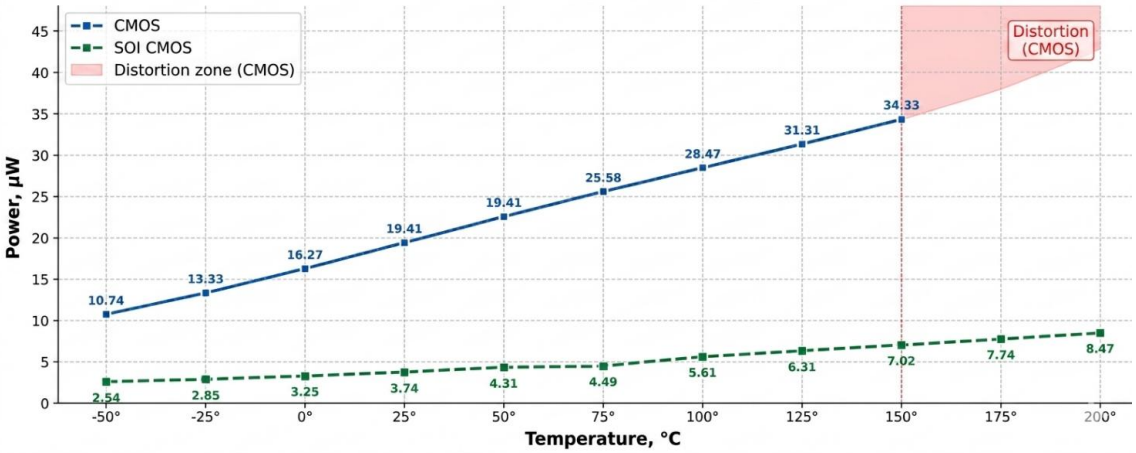

Fig. 4. Comparison of power consumption depending on temperature for CMOS and SOI CMOS ADS.

Conclusions.

1. Comparative analysis of technologies: A comparative analysis of analog-to-digital switches implemented using standard CMOS and SOI CMOS technologies (120 nm) was conducted. It was demonstrated that the use of SOI structures completely eliminates the latch-up effect and minimizes body effect influence. This ensures stable linearity for weak signal transmission (in the millivolt range) at a supply voltage of Vdd = 1.2 V.

2. Energy efficiency: The results of computer modeling directly from the topologies showed that the SOI CMOS switch consumes an average of 4.5 times less power compared to the standard CMOS analogue. In particular, at a temperature of 25 °C, the consumption is 3.74 µW versus 19.41 µW, respectively.

3. Temperature stability: A critical performance limit has been established: standard CMOS circuits lose functionality at temperatures above 175 °C due to a sharp increase in leakage currents (nanoampere range). In contrast, SOI CMOS devices retain full performance at temperatures of 200 °C and above, demonstrating leakage currents in the picoampere range.

4. Practical significance: The proposed three-output multilevel switch circuitry using a virtual capacitance of 0.01 pF is optimal for integration into modern precision SoCs. This makes it promising for use in biomedical sensors, image matrices, and data acquisition systems operating in extreme conditions.

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І.Т. Когут, О.Є. Самарчук, А.Ю. Пристайко, Т.І. Комаришин

Порівняльний аналіз КМОН- І КНІ КМОН аналогово-цифрових комутаторів для мікросистем-на-кристалі в екстремальних умовах

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У статті досліджується конструкція та продуктивність інтегрованих АЦК для сенсорних МнК. Оскільки сучасні сенсорні системи вимагають високої точності та енергоефективності, вибір напівпровідникової технології стає критичним. Сучасні сенсорні МнК вимагають високоточних та енергоефективних АЦК, здатних функціонувати в екстремальних умовах навколишнього середовища.

Проведено комп'ютерне моделювання з використанням конструкторсько-технологічних норм 120 нм, що враховує паразитні ефекти топології, інжекцію заряду та вплив підкладки. Для забезпечення достовірності порівняння розроблено ідентичні топології для КМОН- та КНІ КМОН-версій пристроїв. Результати моделювання демонструють, що КНІ КМОН-комутатори забезпечують значно вищу лінійність та нижчі струми витоку (пікоампери проти наноампер). Встановлено, що енергоспоживання комутатора на основі КНІ в середньому в 4,5 рази нижче за стандартний КМОН-аналог в інтервалі температур від –50 °C до +200 °C. Крім того, стандартний КМОН-комутатор втрачає працездатність при температурах понад 175 °C, тоді як КНІ-пристрій зберігає повну функціональність до 200 °C.

Отримані дані підтверджують, що КНІ КМОН-структури є оптимальним вибором для МнК, які експлуатуються в екстремальних умовах. Запропонована конструкція три вихідного комутатора ефективно перетворює малі синусоїдальні сигнали в імпульсні, що дозволяє використовувати її у біомедичних сенсорах та схемах переносу заряду.

Ключові слова: КНІ КМОН технологія, аналого-цифровий комутатор, мікросистема-на-кристалі, ін'єкція заряду, споживана потужність, високотемпературна електроніка, 120-нм техпроцес.