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Peculiarities of Forming of Microwave Arsenide-Gallium Submicron Structures of Large-scale Integrated Circuit

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The peculiarities of technological processes of formation of submicron Schottky field transistors using arsenide-gallium technology, i.e. the technology of Schottky field transistors formation with a self-alifned gate on the basis of nitride or silicide of tungsten, are considered in the paper. A highly effective technology for the formation of capsular layers of AlN and BN nitride films by high-frequency magnetron sputtering of the proper target in nitric plasma for the realization of GaAs-based MOS-transistors is developed.

Keywords: gallium arsenide, Schottky field transistors, tungsten nitride, tungsten silicide, monocrystalline silicon.

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Introduction

Today Schottky field transistors (SFTs) are the main active elements of GaAs chips of the microwave range. The main purpose of their development is to increase the speed. Digital GaAs integrated circuits/large-scale integrated circuits (ICs/LSICs) belong to the class of ultra-high-speed ones, while analogue devices are generally designed to operate in the microwave range. The following advantages of GaAs compared to mono-Si are used in the development of SFTs and chips on their basis: higher electron mobility in weak electric fields and saturation velocities in strong fields; greater band gap widths and, consequently, a much higher specific resistance of unalloyed gallium arsenide, which allows to form semi-insulating (local and interlayer) layers in the LSIC-structures. However, GaAs is inferior to mono-Si for a number of parameters that are important for the formation of chips. In particular, the high density of surface states in MOS-structures of gallium arsenide does not allow it to form high-quality MOS-transistors and chips, low mobility of holes and small charge time of current carriers makes it difficult to develop bipolar complementary transistors. In this regard, the optimal active element, which allows to realize the advantages of GaAs in the IC/LSIC-structures, compared to mono-Si, is the field-effect transistor with the metal-semiconductor barrier.

I. Peculiarities of technology forming of SFT-structure

One of the first technologies for the formation of structures of arsenide-gallium SPTs is shown on Fig. 1.

The transistor is formed on the substrate 1 of the negative gallium arsenide, which has a slightly degenerate conductivity of *p*-type. To reduce it, when GaAs single crystals are grown by Czochralskiy method, chromium atoms are introduced in small amounts, which compensate the acceptors action. GaAs substrates made from such monocrystalline ingot have an increased static resistance and are called semi-insulating ones.

A highly doped n^+-type source-drain regions 2 and more thin layer of *n*-type channel 3 are formed near the substrate surface 1 by the ion-doping method. The typical thickness of the layer 3 d_0 = 0.1-0.2 μm, and the concentration of donors in the channel N_{dc} = (1-2)·10^{17} cm^{-3}. Ions of silicon (Si^+), selenium (Se^+), and sulfur (S^+) are usually used as doping donor admixtures. Metallic electrodes of gate 4 (for example, in the form of Ti-W alloy) are deposited on the substrate surface above the layer 3. Metallic electrodes 5, for which the gold-germanium composition (AuGe-12) is used, provide contacts to source and drain. A dielectric layer 6 (SiO_2) is deposited on the surface of the substrate that is not in use. The metal gate electrode forms with a layer 3 a rectifying contact (the Schottky barrier), the typical

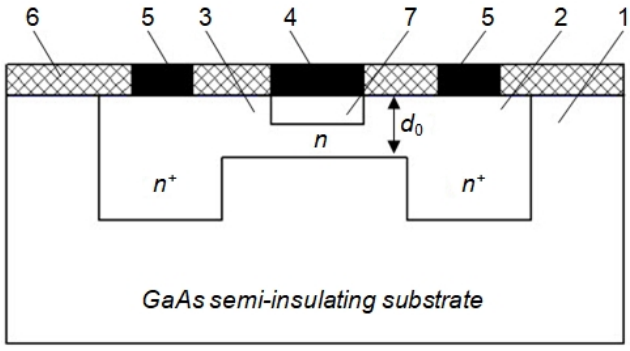

Fig. 1. Structure of the Schottky field transistor.

equilibrium height of which is φ_b = 0.7-0.8 V. The conductive channel between the source and drain is placed in layer 3. It is limited to the top of the depleted region 7 of Schottky barrier and from the bottom – substrate 1. The thickness of the conductive channel is equal to the thickness of the depleted region 7. Typical source-drain distance L = 1.3 μm, the gate length is 0.5-1 μm. The operation principle of SFT is as follows.

The control voltage U_{gs} is applied between the gate and the source, and on the drain - the positive one U_{ds} is applied to drain. When the control voltage changes, the thickness of the depleted layer 7 $L_{dep}(U_{gs})$, the thickness of the conductive channel $d_c(U_{gs}) = L_{dep}(U_{gs})$, its conductivity and the drain current changes too. If the gate voltage is equal to the threshold one U_T, then the depth of the depleted layer 7 reaches the insulating substrate 1 (the channel thickness and the drain current are equal to zero). Threshold voltage is determined from the condition $L_{dep}(U_T) = d_0$:

$$U_T = j_b - \frac{q N_{dc} d_0^2}{2 e_0 e},$$

where φ_b – the equilibrium height of the Schottky barrier (the metal-semiconductor contact), ε_0 – the relative permittivity of GaAs (ε_0 = 13.1). The necessary threshold voltage is achieved by choosing the donor concentration in the channel and the thickness of the layer 3. For example, U_T = -2 V when φ_b = 0.8 V, $N_{dc} = 10^{17}$ cm^{-3}, and d_0 = 0.2 μm. The initial voltage can be positive for a small thickness of the channel d_0. In particular, U_T =0.08 V at d_0 = 0.1 μm with the same concentration of donors in layer 3. In gallium arsenide chips SFTs are used, for which the threshold voltage U_T = -2.5 ÷ +0.2 V. If $U_T < 0$, then the channel is conductive at U_{gs} = 0. Such SFT are called normally open – it is analogous to a MOSFET-transistor with a built-in channel. At $U_T > 0$ and U_{gs} = 0 the channel overlaps with layer 7 and the transistor is called normally closed – it is analogous to the MOSFET-transistor with the induced channel. As we can see, changing the concentration of the donor admixture in the SFT channel by the ion implantation, it is possible to form complementary SFTs and build on this basis high-speed digital LSICs, an order of magnitude more speed than on silicon basis. Thus, changing the retrograde multi-charge donor admixture (Si^{++}, Se^{++}, S^{++}) of channel, it is possible to change the threshold voltage in a high accuracy in the range from -2.0 to +2.0 V. Thus, this is the originality of the arsenide-gallium technology [1].

Fig. 2 shows the drain-gate characteristics of normally open (enriched) 1 and normally closed (depleted) 2 SFTs.

For normally open SFT the control voltage of the gate, at which the drain current flows, can vary from negative voltages (-2.5 V) to positive ones (+0.6 V). This voltage can be increased to +2.0 V by multi-charge combined implantation of light and heavy ions. There is a current in gate circle at high positive voltages at the gate (more than 2.5 V), since the barrier metal-semiconductor opens. Therefore, this barrier is also advisable to increase to a value of 1-1.2 V. As a result, the drain current is limited by the value of $I_{d\ max1}$, which corresponds to the gate voltage $U_{gs\ max}$. For normally closed transistors the gate voltage, at which the drain current flows, is positive and can vary within 0-1.6 V. Here, the maximum drain current should be limited to the value of $I_{d\ max2}$. Therefore, $I_{d\ max1} >> I_{d\ max2}$ for SPTs with the same channel size (0.8-1.2 μm).

Normally closed SFTs are the most promising for GaAs. It is necessary to ensure that the threshold voltage dispersion is as low as possible at forming such transistors. Reducing such threshold voltage dispersion presents today a serious technological problem for multi-charge retrograde ion implantation, since this voltage is linearly or quasilinearly depends on the concentration of donors in the channel and quadratically on the layer thickness.

Both normally open and normally closed SFTs are

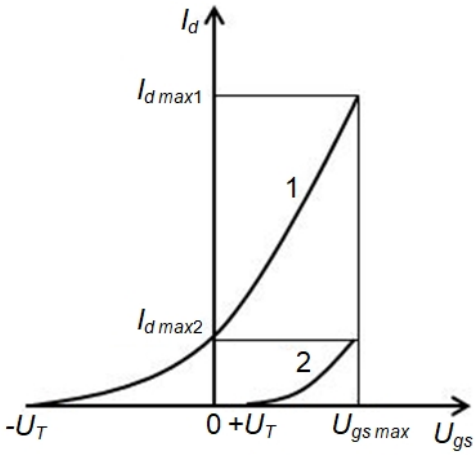

Fig. 2. Drain-gate characteristics of normally open (1) and normally closed (2) SFT.

Table 1

Comparative electrophysical parameters of GaAs and Si

No.	Parameter	GaAs	Mono-Si
1	Mobility, $cm^2/V \cdot s$ at donor concentration 10^{17} cm^{-3}		
	- electrons	$4\text{-}5 \cdot 10^3$	$0{,}8\text{-}1 \cdot 10^3$
	- holes	250-300	350-400
2	Saturation velocity in in a strong electric field, cm/s	$2 \cdot 10^7$	$0{,}8 \cdot 10^7$
3	Maximum resistivity of non-doped material, Ohm·cm	$10^7\text{-}10^9$	10^5
4	Lifetime of of minority charge carriers, s	10^{-5}	10^{-3}
5	Density of surface states of MOS-structures, cm^{-2}	$10^{12}\text{-}10^{13}$	$10^{10}\text{-}10^{11}$

Table 2

Electrophysical parameters of test structures of GaAs SFT

No.	The electrophysical parameter of SFT-structure	Parameter value
1	Donor concentration in channel, cm^{-3}	$(1\text{-}3) \cdot 10^{17}$
2	Mobility electrons in channel, $cm^2/V \cdot s$	$(4\text{-}5) \cdot 10^3$
3	Channel thickness, nm	50-200
4	Schottky barrier hight, V	0.7-0.85
5	Gate length, μm	0,5-1
6	Gate width, μm	3-15
7	Source-drain distance, μm	1-3
8	Channel length of transistor, μm	10-12
9	Threshold voltage, V	
	- normally open transistor	-(2.5-0.5)
	- normally closed transistor	0-1.2
10	Steepness per channel width unit, mS/mm	100-150
11	Specific capacity, pF/mm	
	- gate-source	0.5-1.5
	- gate-drain	0.1-0.2
	- drain-source	0.05-0.1
12	Limit frequency, GHz	60-90

used in complementary chips. Such circuits have minimum power consumption only at switching points. It is necessary to perform additional technological operations for their formation in one crystal. One of the technology options is to etching the part of *n*-type layer 3. Then normally open SFTs are formed in thicker *n*-type layer, and normally closed ones – in more subtle layer. Recent transistors are also called transistors with a deep gate. In the second variant, two operations of ionic selective doping by multicharge (light and heavy) ions are used, with the help of which the *n*-type regions for the various SPTs are formed successively.

For transistors with a long channel ($L > 1$ μm), the steepness of SFT is described by the expression:

$$S = \frac{b\, m_n\, e_0\, e_n (U_{gs} - U_T)}{L_0\, d_0},$$

where b – channel width, L_0 – effective channel length. Thanks to the higher mobility of electrons ($4\text{-}5 \cdot 10^3$ $cm^2/V \cdot s$) the steepness value is much higher than in silicon MOS-transistors at the same size. Unlike mono-silicon, gallium arsenide is characterized by a lower critical electric field strength ($3 \cdot 10^3$ V/cm), at which the drift velocity reaches its saturation. Therefore, the effect of strong field appears at a greater channel length and drain voltage in GaAs SFT, than in silicon one. Table 1 shows for comparison the basic electrophysical parameters of GaAs and Si at $T = 300$ K.

In transistors with a short channel ($L < 0.8$ μm), the drift velocity reaches saturation, the drain-gate characteristic is close to the linear one, and the steepness depends weakly on the gate voltage and is determined by the expression:

$$S = e_0\, e_n\, d_{sat} / d_0 .$$

Thus, the greater steepness of GaAs SFT compared to silicon MOS-transistors of the same size is due to a higher saturation velocity of $2 \cdot 10^7$ cm/s.

Unlike silicon MOS-transistors with induced channel, GaAs SFT have very small parasitic gate-source and gate-drain capacities since the gate does not overlap region 2. In addition, there are drain-substrate and source-substrate barrier capacities, since the substrate is semi-insulating – the concentration of admixtures is

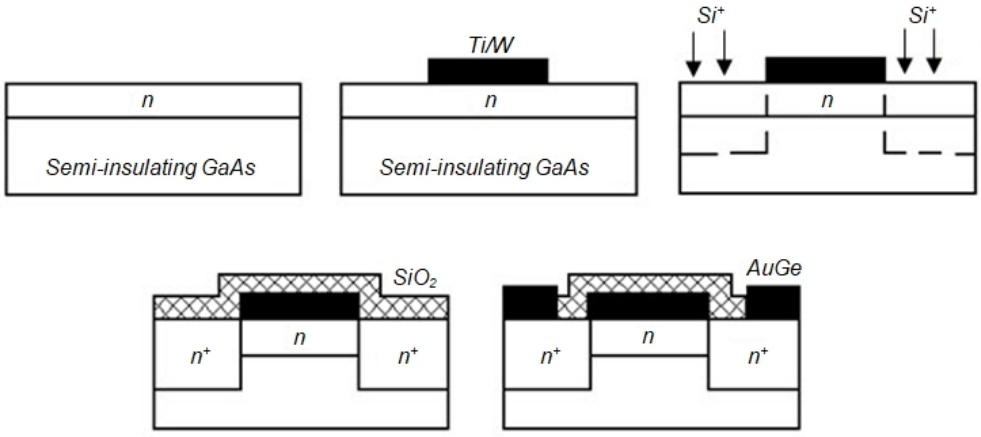

Fig. 3. Technological process of forming of self-aligned SFTs on the GaAs semi-insulating substrates.

small, and the thickness of the depleted n^+-region and transitions is large. Only the gate-channel capacity $C_{gc} = e_0 e_n b L_g / L_{dep}$, which is the barrier capacitance of the metal-semiconductor contact transition, has a significant value. At the voltage $U_{gs} > U_T$ it is calculated by the above formula. To reduce this capacity, it is necessary to reduce the length of the channel (L < 0,6 μm), which increases the SFT speed [2].

The limit frequency of steepness is determined by the transit time t_{tr} of the of electrons through the channel at a small length of the gate channel $t_{tr} = L_g / u_{eff}$, i.e. $f_s = u_{eff} / 2p\, L_g$, and f_s > 60 GHz when L_e = 0.5μm.

When SFT is worked in pulsed mode, its switching time is determined by the transit time of electrons through the channel and the recharge time of the loading capacity. Increasing of speed of GaAs digital chips compared to silicon ones is due to an increase in the steepness of SFT, as well as a decrease in the transit time of the electrons and parasitic capacitors of the transistors. Therefore, to increase the steepness of SFT, a self-aligned technology with a gate was developed.

Table 2 shows typical electrophysical parameters of the test structure of SFT with the structure depicted on Fig. 1.

Consider the structure of SFT with self-aligned gate, the main technological processes of which are shown at Fig. 3.

The SFT-structure is formed on a semi-insulating GaAs substrate, where *n*-layer of 0.08-0.1 μm in thickness is formed by selective ionic doping of substrate with silicon (Si^{++}) through SiO_2 mask. The SFT channel is located in this layer, on the surface of which the gate is formed. The gate of the transistor represents a strip of tungsten silicon of 0.8 μm in length. Tungsten silicon is chosen as a gate to withstand a photonic treatment at 700°C for resistance reducing.

Selective epitaxial growth by vapour-chemical reactions from metal-organic compounds or molecular-beam epitaxy is used at the formation of n^+-type drain-source regions. Then, a dielectric SiO_2 layer is deposited and photonic annealing is carried out to activate and reduce radiation defect, which leads to a significant increase in the mobility of charge carriers. Plasma-chemical etching opens the windows for the contacts in the insulator and the contacts to the drain-source regions are formed by deposition a metal layer from AlGe-12 alloy using ion milling [3].

The following electrophysical parameters were obtained for SFT with self-aligned gate at L_g =1.5μm and b = 1 mm: U_T = 0.6 V, R_{load} = 0.75 Ohm, S/b = 87 mS/mm. Compared to SFT formed without self-aligning of the same size, the source resistance decreased by 5-8 times, and the steepness increased by 3-5 times. In a structure with a self-aligned gate, the breakdown voltage at the gate is determined by the concentration of admixtures in the n^+-regions, as they adhere to the gate.

The maximum donor concentration in n^+- regions is $7 \cdot 10^{17} \div 1 \cdot 10^{18}$ cm^{-3} and the breakdown voltage of the gate is 6-10 V at ion energy 150 eV and dose $(1.7\text{-}2) \cdot 10^{13} cm^{-2}$. The disadvantage of such a structure with a self-aligned gate is a slightly increased parasitic gate-source and gate-drain capacitances, which can be reduced by using high-resolution lithography [4].

Conclusions

1. Submicron self-aligned technology for the formation of complementary SFTs on GaAs for the high-speed structures of LSICs are developed.
2. A highly effective technology for the formation of capsular layers of AlN and BN nitride films by high-frequency magnetron sputtering of the proper target in nitric plasma for the realization of GaAs-based MOS-transistors is developed.
3. The technology of formation of epitaxial buffer layers of germanium for the alignment of lattice constants of GaAs and GaAsAl semiconductor materials on mono-Si are developed and studied for the realization of reliable hetero-junction.

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Особливості формування НВЧ арсенід-галієвих субмікронних структур великих інтегральних схем

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У роботі розглянуто особливості технологічних процесів формування субмікронних польових транзисторів Шотткі з використанням арсенід-галієвої технології, а саме технологію формування польових транзисторів Шотткі із самосуміщеним затвором на основі нітриду або силіциду вольфраму. Розроблено високоефективну технологію формування капсулюючих шарів нітридних плівок AlN та BN високочастотним магнетронним розпиленням відповідної мішені в азотній плазмі для реалізації МДН-транзисторів на GaAs.

Ключові слова: арсенід галію, польові транзистори Шотткі, нітрид вольфраму, силіцид вольфраму, монокремій.