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Design of SOI transistors taking into account the influence of a floating body and a controlled base

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The paper proposes an alternative technology that uses a transistor body modification, whereby a larger modification provides increased device current during switching, while the slope reduces leakage current during storage. The body influencing methods improved performance, especially in the low voltage range.

A technology has been developed that can be used to address low voltage operation without any loss in speed or increase in source leakage. Alternatively, it can be used to speed up the operation of the circuit without any increase in power consumption. The proposed structure starts with an n-gate MOSFB, which is particularly attractive and widely used with SOI substrate technology. Unlike the conventional, source-bound layout style, the n-gate layout style uses polysilicon gate extensions, parallel, on both sides of the channel, to create an isolated contact between the element surfaces.

Keywords: MOS transistor, SOI, floating body, subchannel region, signal.

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Introduction

Currently, the rapid development of electronics is causing the emergence of new technologies for creating and designing SOI transistors. The process of manufacturing SOI-MON floating-body transistors begins with the creation of active regions in the silicon layer of the device, which will ultimately contain the source, drain, and gate of the transistor [1-3]. These active regions are created by removing excess silicon through a photolithographic process that serves to isolate the individual active regions from each other. The voids in the device layer created by the photolithographic process are filled with silicon dioxide to restore a flat surface on the substrate.

The proposed structure starts with an n-gate MOS transistor, which is particularly attractive, being widely used with SOI substrate technology. Unlike the conventional, source-bound layout style, the n-gate layout style uses polysilicon gate extensions, parallel, on both sides of the channel, to create insulated contacts between the element surfaces.

Using these contacts, independent body tilt can be applied to individual devices in a partially depleted SOI circuit. [4-5]. In general, the analysis of literature sources and the state of the problem showed the relevance of this topic and the need for further scientific and applied research to improve the design of SOI MOS transistors with a floating body.

I. Properties and approaches to the design of floating-body SOI MOS transistors

For SOI devices, the body of each device is independent from the base oxide layer, the drain regions effectively isolating adjacent transistor body regions from each other. Therefore, to control the transistor body voltage, it is necessary to communicate on an individual basis. While there is no risk of defects, to eliminate defects from the MOSFB, the body voltage can increase, changing the characteristics of the device.

To obtain uniform device features, special attention must be paid to body defects. The general approach is to

connect the body to the output side of the transistor using a P+ insertion next to the N+ source [6].

While an n+/p+ junction would typically form a diode, a further step is used to reduce the gate resistance. The introduction of both sides of the channel also moves the transistor channel inward from the silicon active edge – the moving source-source, conductive tracks away from the silicon edge prevent transistor edge effects from affecting the device's operation. The width of the transistor is determined by the distance between the output coupling and the input at each end of the channel.

A transistor design with an independent contact between the element surfaces is shown in Figure 1. Unlike the source-bound design, a polysilicon segment is placed between the source and body junctions to prevent silicide from bridging the junction. This creates a diode between the source and body, and keeps the body as an independent node with a bias independent of the output voltage.

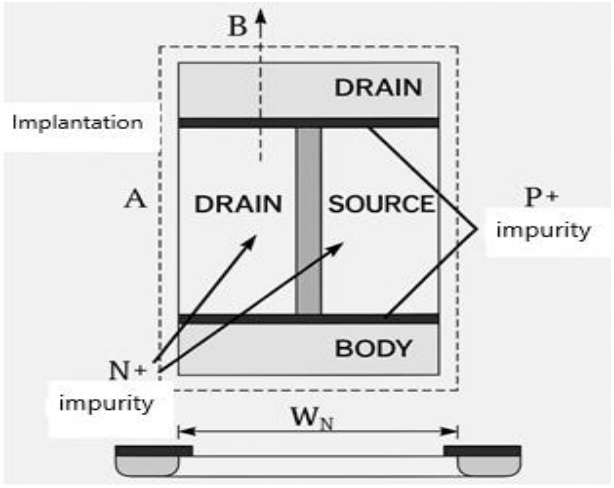


Fig.1. SOI MOSFT with independent contact between the surfaces of the elements.

For this design, if the body is left unconnected, the body tilt will float as a function of the drain [7]. This can cause the characteristics of the transistor to change.

Alternatively, the designer can directly bond the active regions to the body to act on these nodes independently. In this case, the transistor width is fixed because the spacing between the multi-silicon segments would normally isolate the contacts between the element surfaces.

Compared to a source-bound arrangement, the width is effectively reduced by one gate length because the polysilicon blocks part of the source insertion.

II. Results of simulation of SOI of floating-body MOS transistors.

To characterize the effect of body displacement on individual devices, many types of devices have been investigated. This compact yet effective set of devices can be used to verify existing models, especially at low voltages, under variable displacement conditions, the effects of design choices at work.

Drain-coupled devices are included with variations in width (ranging from 10μm to 2.4 μm), length (from 1.20 μm to 0.50 μm) to determine the electrical width, length (W_{EFE}, L_{EFF} respectively) for the process. For devices with independent contact between the element surfaces, L_{EFF} will be similar to source-coupled, but W_{EFF} will be different because other physical features determine W_{EFF}. For independent surface-to-surface contact devices, another set of variable width transistors (10 μm to 2.4 μm) was developed to investigate the W_{EFF} transistors exhibit with polysilicon surface-to-surface contact isolation [8].

Micrographs of the transistor are shown in Figure 2.

The electrical results, analysis are shown in Figures 3

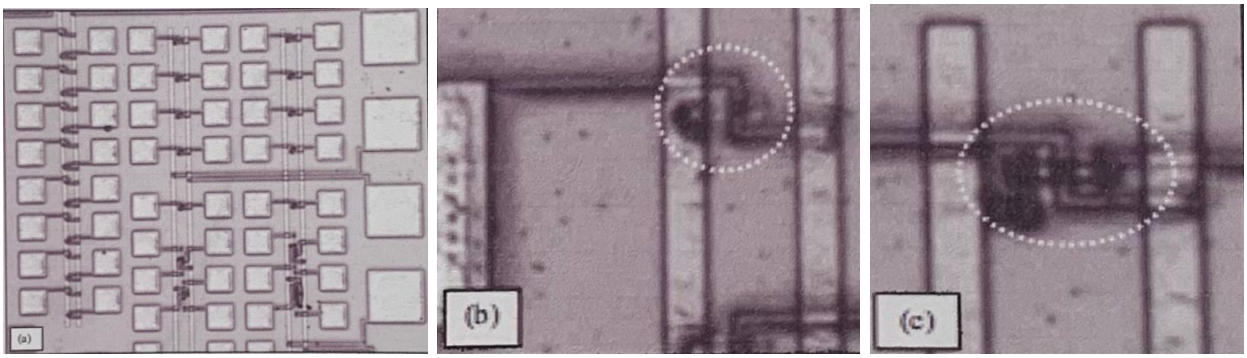


Fig.2. Micrographs (a) for testing transistors and their structure, (b) MOSFET with a tied source of contact between the surfaces of the elements, (c) with an independent contact between the surfaces of the elements.

Table 1.

Brief overview of transistor structures for testing.

Width replacement, the source is connected and independent under the channel area		Width replacement, only connected drain	
W (nm)	L (nm)	W (nm)	L (nm)
W=10 nm	L=0,5 nm	W=10 nm	L=0,5 nm
W=5 nm			L=0,6 nm
W=4 nm			L=0,8 nm
W=3 nm			L=1,2 nm

to 5. The display of Figures 3, 4 records the results of the ID-vgs for nominal n-MOS, p-MOS devices - transistors.

The features of the VAC characteristics give many parameters of transistors. Of particular interest are those that affect the physical design of the device, its use in certain key studies intended in this project. Among these device parameters are such as the effective gate length, the effective channel width.

Effective gate length is the electrical gate length, which can vary from a certain length due to the propagation of junctions below the gate, changes in impurity concentrations, and changes in the gate-level photolithography process.

The difference between analytical, electrical measurements for length, width can be obtained from the characteristic of resistance, conductivity versus width, length. The total resistance of the series - including the probes, contacts, resistance of the connections - is 85Ω. As shown in Figure 5, the curves converge at - 0.4 μm, so adjusted to be 0.4 μm, the electrical width is slightly larger than the drawn width. Since the actual device width is determined by individual doping steps determined with individual photolithography processes, it is likely that the interaction between the n+ insertion, which forms the source width, and the p+ width, which forms the body junction, could have resulted in a variation in the device width from the nominal value.

For example, junction concentration, depth, as well as misalignment between lithographic steps, can affect the width.

Deviations from the analytical measurements of the device can affect the measuring transistor as the electrical representation of the offset is off-valued.

III. Discussion of the results and prospects for the development of the method

Thus, having examined in detail the technology of creating SOI-MON transistors with a controlled base, we come to the conclusion that transistor structures based on SOI show high technological characteristics with relative simplicity of production.

The technology of manufacturing SOI substrates is considered, this technology is an example of technologically complex substrates, designed mainly to increase the speed of transistors. This technology is becoming more and more developed in leading companies in the world, it allows the creation of partially or fully depleted transistors with high speed, with lower loss currents and power consumption.

Special attention is paid to the design of SOI transistors taking into account the influence of the floating body and the controlled base. The properties of SOI-MOS transistors with a floating body and approaches to their design were also characterized.

Therefore, the proposed structures based on SOI and the MOS transistors with a controlled base manufactured on them are an evolutionary step in the development of the production of circuits and devices for microsystem technology.

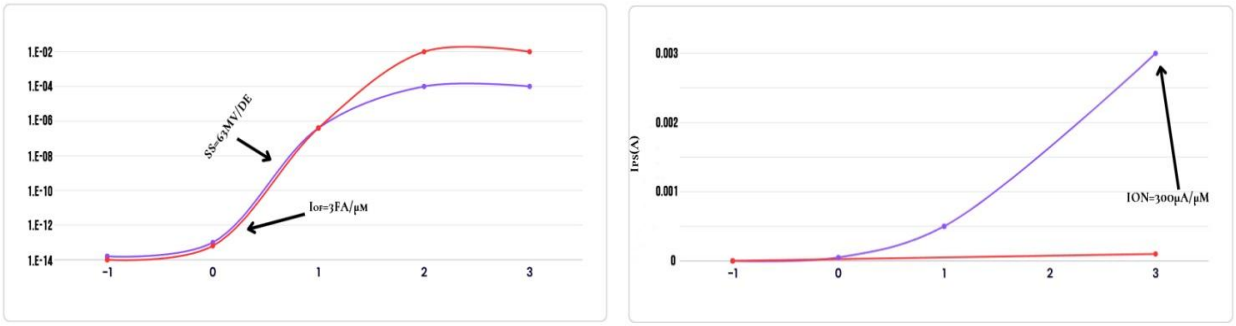


Fig. 3. Input voltage features of the SOI MOS transistor, W/L= 10μm/0.5μm. (a) for V_{DS}=0.05V, 3V. (b) VT at the output VIDS-VGS to VDS.

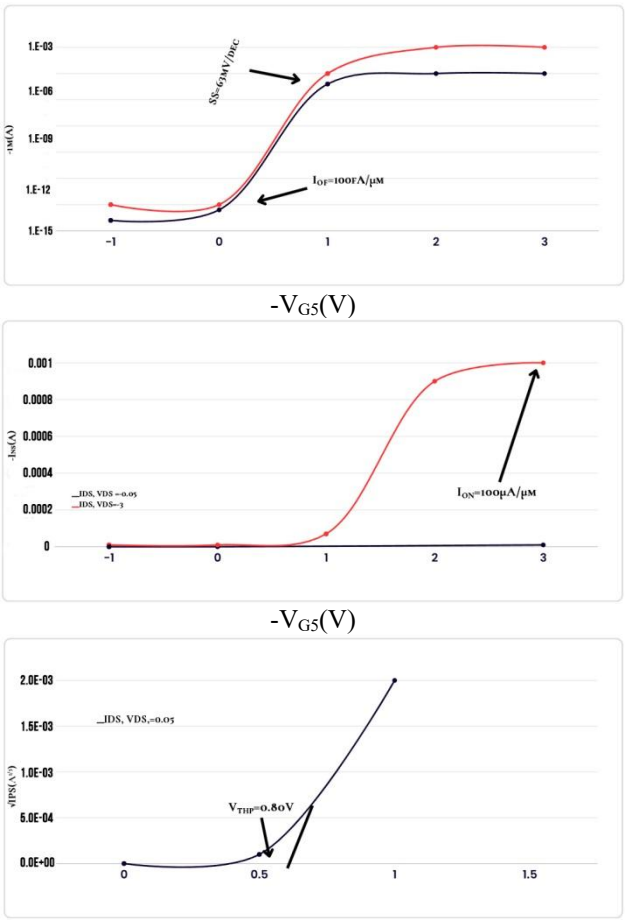
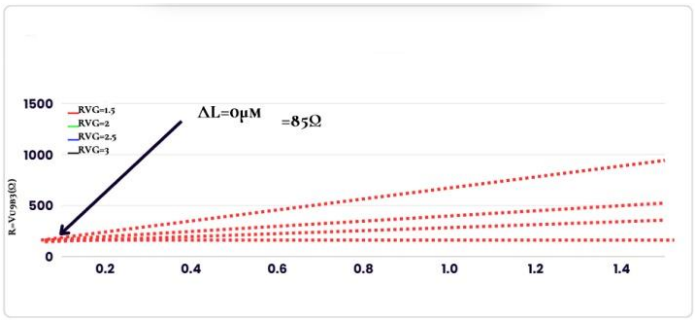


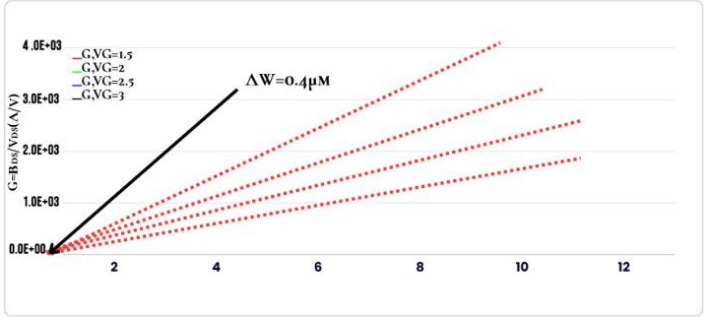
Fig. 4. Input voltage features of the SOI MOS transistor, WL=10μk/0. 5μm. (a) for VDS=0.05V, 3V. (b) VT at the output VIDS-VGS to VDS.

Calculation of ΔL



FET width (mm)

Calculation of ΔW



FET width (μm)

Fig. 5. Transistor parameters with VAC dependences. (a) Function of transistor length. (b) Function of transistor width.

Conclusions

The existing principles and methods of designing SOI transistors taking into account the floating body and the controlled base are analyzed, and ways of their improvement are shown to increase efficiency and expand the number of parameters obtained by this technology.

A technology has been developed that uses a transistor body shift, whereby a larger shift provides increased device current during switching, while a slope reduces leakage current during storage.

It has been proposed that the use of transistors with independent contacts between the element surfaces allows the designer to vary the operation of the device for given gates. If the body is left unbonded, the body bias will float as a function of the drain. This can cause the transistor characteristics to change. Alternatively, the designer can directly bond the active regions to the body to affect these nodes independently. In this case, the width of the transistor is fixed because the spacing between the polysilicon segments would normally isolate the contacts between the element surfaces. Compared to a bonded source arrangement, the width is effectively reduced by one gate length because the polysilicon blocks part of the source insertion.

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Проектування КНІ-транзисторів з врахуванням впливу плаваючого тіла і керованої бази

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В роботі запропоновано альтернативну технологію яка використовує зміну тіла транзистора, за допомогою чого більша зміна забезпечує збільшений струм пристрою під час перемикання, тоді як нахил зменшує потік витоку під час зберігання. Тіло, що робить вплив на методи поліпшило роботу, особливо в низькому діапазоні напруг.

Розроблено технологію, яка може використовуватися, щоб вирішити низьковольтну операцію, без будь – якої втрати в швидкості, або збільшення джерела витоку. Альтернативно це може використовуватися, щоб прискорити роботу схеми без будь якого збільшення витрат енергії. Запропонована структура починається з МОНПТ з n-затвором, який особливо привабливий і широко використовується з технологією підкладки КНІ. На відміну від звичайного, прив'язаного витоком типу розташування, стиль розташування n-затвору використовує полікремнієві розширення затвору, паралельні, з обох боків каналу, щоб створити ізольований контакт між поверхнями елементів.

Ключові слова: МОН-транзистор, КНІ, плаваюче тіло, підканальна область, сигнал.