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Short comparative analysis on the prospects for the use of three-dimensional FIN FET transistors for sensor electronics

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The development of modern electronics is based on the introduction of modern micro- and nanoelectronic technologies. Traditional complementary metal-oxide-semiconductor (CMOS) planar transistor structures based on bulk silicon are gradually giving way to more advanced structures with better electrical, frequency, energy characteristics, and radiation resistance based on three-dimensional (3D) "silicon-on-insulator" structures that provide better electrical characteristics, higher speed, energy efficiency with the possibility of further scaling. Promising areas of use for both traditional microcircuits and sensor electronics are the use of 3D nanometer transistors of the FinFET, Gate-All-Around (GAA) type, as well as those based on nanosheets and nanowires. The paper considers the structures of such types of SOI nanometer 3D transistors and examples of their use in sensor electronics.

Keywords: sensor electronics, nanometer structures "silicon-on-insulator", silicon nanowires, FinFET.

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Introduction

Planar integrated transistor structures of the silicon-on-insulator (SOI) type exhibit significantly better characteristics in terms of speed, energy efficiency, integration density, radiation hardness, and other parameters compared to traditional bulk silicon-based planar structures. Various technologies have been used to create these structures, including laser recrystallization of a polysilicon layer on silicon oxide [1], formation of a silicon oxide layer beneath the surface of a silicon wafer via oxygen ion implantation [2], wafer bonding methods [3], smart cut techniques [4], and methods for forming local three-dimensional (3D) SOI structures with predefined topology both on the surface and beneath it within a silicon wafer [5]. Research in this field and the development of microelectronic technologies from micrometer to nanometer scales have led to the creation of new types of nanometer-scale transistors, such as FinFETs (field-effect transistors with a "fin" structure) on bulk silicon, as well as FinFETs with SOI structures and their modifications – for example, multi-gate FinFET transistors, triple-gate (3G) MOS structures, and gate-all-around (GAA) MOS transistors [6]. These modifications provide additional opportunities for the creation of modern nanometer-scale complementary CMOS transistor structures for integrated circuits (ICs), as well as for integrated sensors with monolithic integration into ICs for building sensor-type system-on-chip microsystems.

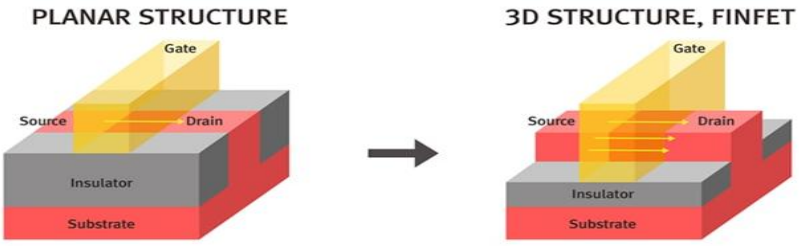
Table 1 presents the basic steps involved in the fabrication of FIN (fin-type) elements, which will form the base of the transistor channel [7]

The main technological operations: photolithography, dry reactive ion etching (RIE), and surface cleaning, each plays a crucial role in ensuring the formation of a precise and uniform transistor structure. As a result, tall silicon fins are formed on the wafer surface, which will subsequently be covered with a gate dielectric and a gate electrode. The dimensions of these fins determine the effective channel length and width of the transistor, which in turn define its electrical characteristics. Figure 1 schematically shows the structures of a (a) planar transistor and b) 3D FINFET.

Table 1.

Basic steps of fin-type element fabrication technology

Step	Description	Method / Materials	Equipment	Purpose
Photoresist coating	Application of photoresist onto the wafer by spin-coating.	Spin-coating of positive or negative photoresist	Lithographic coating equipment (TEL ACT 12, SUSS MicroTec)	Preparation of a mask for precise fin geometry definition
Exposure process	Exposure of the photoresist to UV/DUV light through a photomask that defines fin placement.	Deep ultraviolet (DUV) or extreme ultraviolet (EUV) lithography	ASML, Nikon Stepper	Creating an accurate pattern of future structures
Photoresist development	Formation of a photoresist mask for FIN element definition.	Chemical developer (TMAH) – tetramethylammonium hydroxide, $(CH_3)_4NOH$)	Automatic developer (DNS, TEL Clean Track)	Opening silicon areas for subsequent etching
Anisotropic reactive ion etching (RIE) of silicon	Vertical, controlled ion-plasma etching of silicon to form fins (FINs) of defined dimensions.	Reactive ion etching (RIE) in $Cl_2/HBr/O_2$ or SF_6 ambient	Drytek Quad RIE, Lam Research TCP 9400	Formation of high-aspect-ratio silicon fins with required dimensions
Photoresist removal and cleaning	Plasma etching of the photoresist in oxygen or using chemical solutions. Wafer cleaning from etchant residues.	O_2 plasma cleaning, Piranha solution ($H_2SO_4 + H_2O_2$)	PVA TePla, Gasonics Aura 1000	Surface preparation for the subsequent stages of the technological process



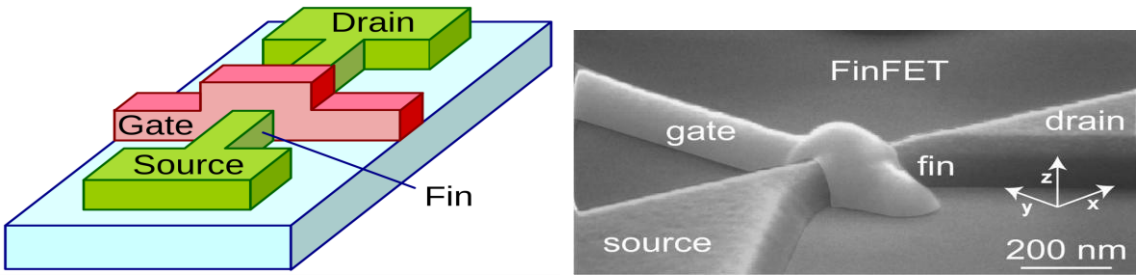
a) b)

Fig. 1. Structures of a) planar transistor and b) 3D FINFET.

The FinFET (Fin Field-Effect Transistor) technology has become a key breakthrough in micro- and nanoelectronics, replacing traditional planar transistors and enabling the necessary levels of scaling and energy efficiency. Thanks to the vertical "fin" structure that protrudes above the substrate and is surrounded by the gate on three sides, the FinFET offers significant advantages in controlling the transistor's conduction channel, reducing leakage currents, and improving the ratio of off-state current (.I_{off}) to on-state current (I_{on}).

The structure of an SOI (silicon-on-insulator) FINFET is shown in Figure 2(a), and Figure 2(b) presents a microphotograph of such a transistor, indicating its electrodes.

The next evolutionary step in the development of FINFET structures is the so-called GAA (Gate-All-Around), transistors in which the gate surrounds the transistor's channel region from all sides—a circular gate—providing even better control over the charge carrier flow in the transistor channel. This further reduces leakage currents compared to FINFET, improves energy efficiency, and ensures higher device performance. GAA transistors can be implemented as nanosheets or nanowires, allowing flexible adjustment of their parameters depending on the requirements of specific microchip elements or sensor devices. The transition from FINFET structures to multilayer GAA transistors is shown in Figure 3 [8].



a) b)

Fig.2. Structure of a 3D FINFET on an insulator (blue color) a) and its microphotograph b).

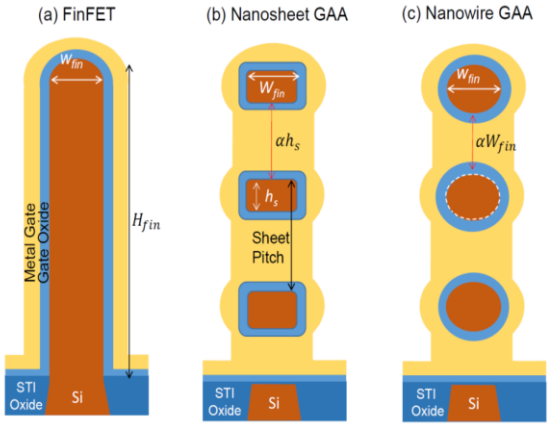


Fig. 3. Cross-sectional views of transistor structures: a) FINFET, b) multilayer nanosheet, (c) multilayer nanowire.

Table 2.

Basic technological steps for forming FINFET and GAA MOS transistor structures [9], [10], [11].

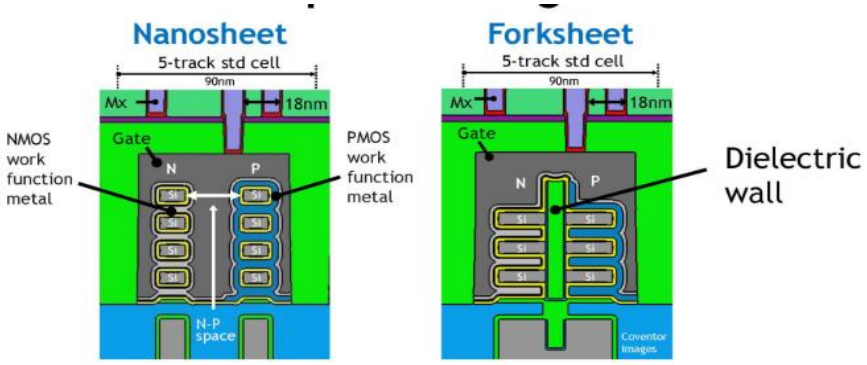
Step	FinFET	GAA
Channel formation	The channel is formed as a fin with two sidewalls.	The channel is formed on all four sides, requiring more precise technologies.
Channel structure creation	The channel has a vertical structure surrounded by the gate on two sides.	The channel is surrounded by the gate on all four sides, adding complexity.
Polycrystalline silicon deposition	Deposition of polycrystalline silicon on the side parts of the fin.	Deposition of polycrystalline silicon around the channel on all four sides.
Lithography for gate masks	Lithography to create masks on the side surfaces of the fin.	Lithography must consider all four sides of the channel to form masks
Channel etching	Etching only the side parts of the channel.	Etching the channel on all four sides, requiring more precise processes.
Ion implantation	Ion implantation on the side surfaces of the channel.	Ion implantation to adjust properties on all four sides.
Rapid thermal annealing (RTA)	Annealing to activate dopants on the side parts.	Annealing for all four sides of the channel for uniform activation.
Low-temperature oxide (LTO) deposition	Deposition for isolation of the side parts of the fin.	Deposition for isolation of the channel on all four sides.
Lithography for contact windows	Lithography for contacts on the side parts of the channel.	Lithography for contacts on all four sides of the channel.
Contact window etching	Isotropic etching for the side parts.	Etching of contact windows on all four sides of the channel.
Metal deposition	Metal deposition on the side parts of the fin.	Metal deposition on all four sides of the channel.
Lithography for metal interconnections	Lithography for metal interconnections on the side surfaces.	Lithography for forming interconnections on all four sides of the channel.
Metal etching	Isotropic metal etching on the side parts of the channel.	Metal etching to clean and stabilize connections on all four sides.
Annealing	Annealing to improve contacts on the side parts.	Annealing to improve contacts on all four sides of the channel.

The difference in the fabrication technology of FET and GAA structures is presented in Table 2.

A further development concept within GAA technologies is the forksheet channel structure, where the channel branches into several parts, providing a larger surface area for the gate region. This design enables improved electrostatic control and reduced leakage currents, as the increased channel surface can conduct more current without increasing the chip area.

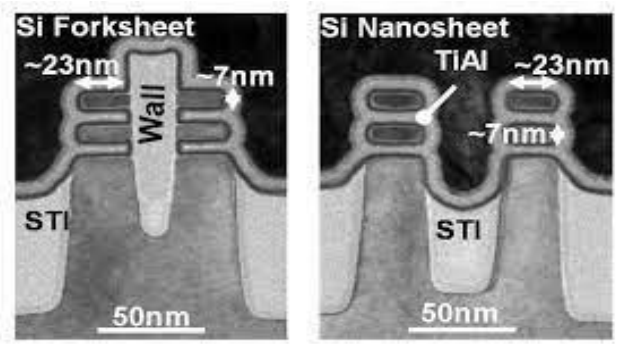
The cross-sectional views of the Nanosheet and Forksheet structures are shown in Figure 4, and the photographs of their cross-sections are shown in Figure 5.

The comparative properties of different SOI transistor architectures are presented in Table 3.



a) b)

Fig. 4. Schematic cross-sectional view of Nanosheet a) and Forksheet b) SOI nanostructures.



a) b)

Fig. 5. Cross-sectional micrographs of Forksheet a) and Nanosheet b) SOI nanostructures.

Table 3.

Comparative properties of SOI transistor architectures.

	Silicon-on-Insulator (2000-2010s)	**FinFET (5 nm) (2015-2020s)**	**Nanosheet (GAA) (2023-2030s)**	**Forksheet (2025-2030s)**
Architecture	Silicon on an insulator layer to reduce parasitic effects	Three-sided gate control around the channel (channel open at the bottom)	Full gate control around the channel (360-degree surround)	N- and P-transistors separated by a dielectric wall for denser placement
Transistor density	~10 million transistors/mm²	~150 million transistors/mm²	~200 million transistors/mm² and more	Higher than nanosheet due to tighter layout
Power consumption	Supply voltage ~1.0–1.2 V	Supply voltage ~0.65 V	Supply voltage ~0.5 V	Lower than nanosheet due to improved layout
Scalability	Limited to ~22 nm	Down to ~3 nm	<3 nm (expected for 2 and 1 nm)	Optimized for sub-2 nm² technology
Area efficiency	Improved, reduced area (~500 nm²)	High, area per transistor ~50 nm²	Very high, effective area ~40 nm² or less	Less than 40 nm²
Application	Biosensors, MEMS, accelerometers	Smartphone sensors, 3D cameras, image sensors, LiDAR	High-precision IoT sensors, quantum sensors, biomedical implants	Ultra-high resolution sensors, neuromorphic sensors for AI, sensors for autonomous

I. Examples of SOI nanostructure applications in sensor electronics

One potential application of three-dimensional transistors in sensor electronics is the hybrid thermal sensor shown in Figure 6 [12]. It is implemented using 22-nm FinFET technology based on n-channel MOS transistors operating in the subthreshold regime with a parasitic PNP transistor. The sensing system achieves an accuracy of ±1.07 °C and occupies an area of 4.3 μm². It consumes 50 μA of current from a 1 V power supply.

Another example of using such transistors in sensors is the current-splitting magnetic sensor [13], which is fully compatible with FinFET technology based on silicon-on-insulator (SOI). The fabricated device, featuring a double gate and four contacts, offers a revolutionary advancement in the capabilities of integrated SOI sensors, with a measured sensitivity Sr of approximately 30% at a total supply current of 2 μA.

The study [14] investigates the influence of the channel length of a FIN FET transistor based on $Si_{0.25}Ge_{0.75}$ as the semiconductor material on the thermal sensitivity and performance of FIN FET transistors. The FinFET structure demonstrates an enhanced gate control and improved suppression of short-channel effects.

This study examines the impact of thermal sensitivity on the performance of FinFET transistors, focusing on the role of varying channel lengths in improving electrical characteristics. With the advancement of semiconductor technologies, understanding the influence of temperature on electronic devices becomes crucial for ensuring their stability across different applications. Semiconductor manufacturing follows Moore's law, which requires reducing transistor sizes to increase integration and reduce costs. However, biosensors with conventional planar transistors are sensitive to short-channel effects, leading to increased power loss and reduced sensitivity.

The FinFET structure demonstrates enhanced gate control and improved suppression of short-channel effects. The study employs modeling methods to analyze the current-voltage (I-V) characteristics of the FinFET structure, which uses $Si_{0.25}Ge_{0.75}$ as the semiconductor channel material. The influence of different temperatures (275, 300, 325, and 350 K) was analyzed with channel lengths of 10, 20, and 30 nm, focusing on the change in current (ΔI) within an operating voltage range from 0 to 1 V (VDD).

The results show that thermal sensitivity increases as the channel length decreases, particularly between 10 and 20 nm, where the optimal length is 20 nm due to a balance between low threshold voltage and reduced drain-induced barrier lowering (DIBL), while maintaining stable operation within the studied temperature range. The study also showed that the device operates effectively at a drain voltage (Vd) of 0.9 V, providing stable performance between 325 and 350 Kelvin.

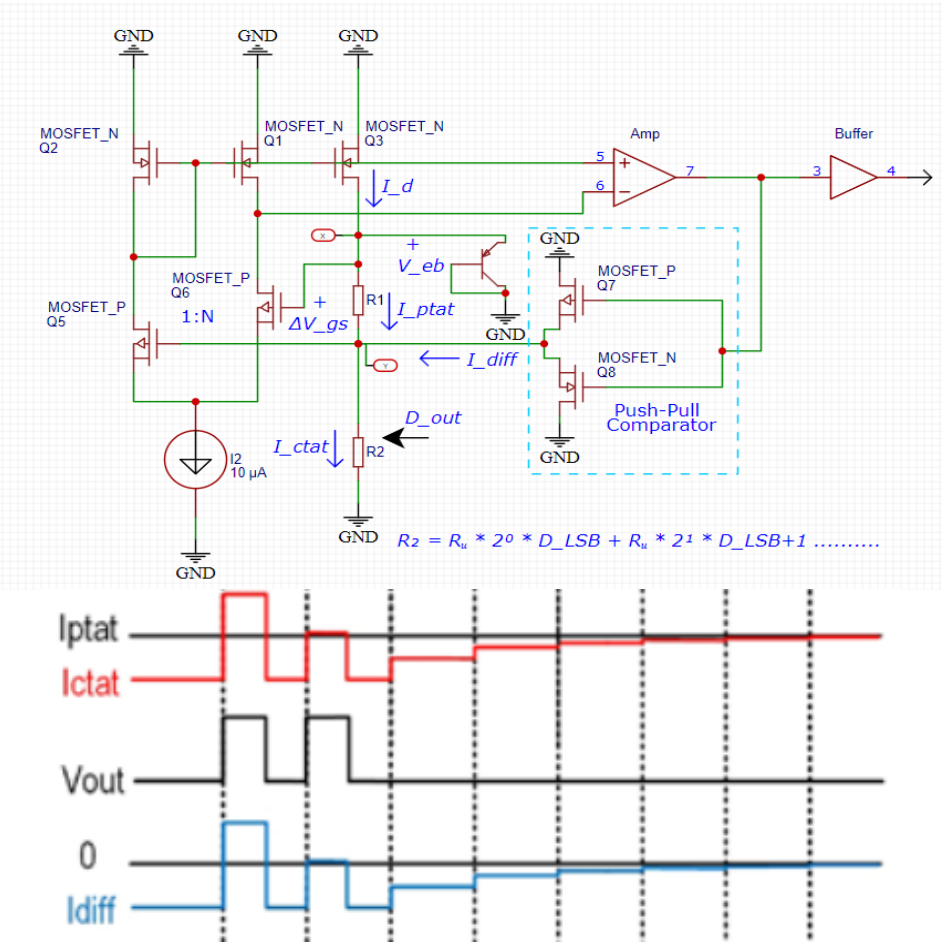
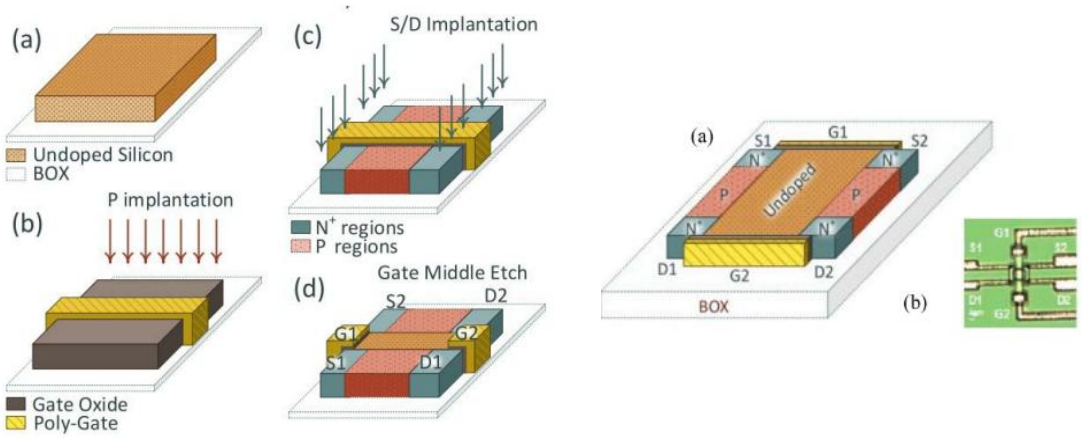
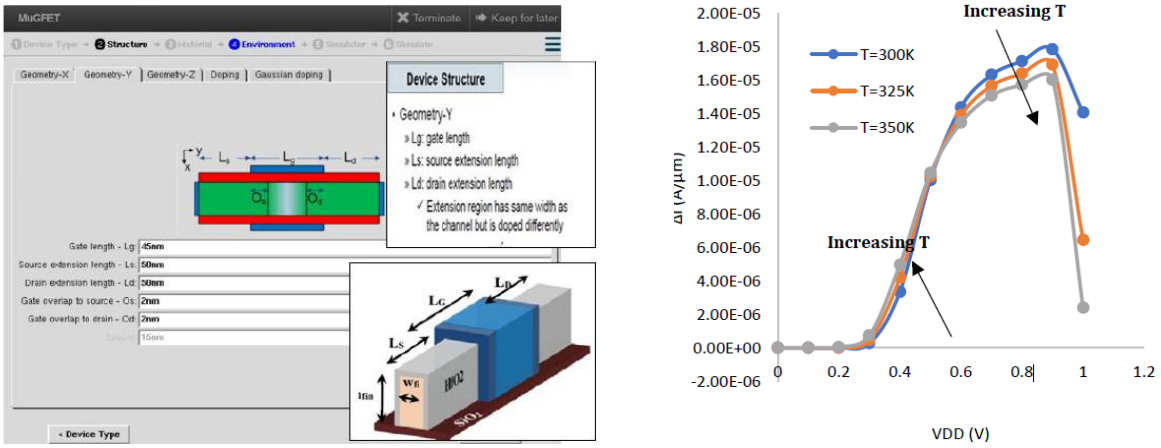


Fig. 6. Example of a hybrid thermal sensor based on an n-channel MOS transistor.



a) b)

Fig. 7. Basic steps for fabricating a magnetic sensor on SOI structures a) and its design b).



a) b)

Fig. 8. Modeling results of a) the influence of FinFET transistor channel length and b) temperature on the transistor I-V characteristics.

These findings highlight the importance of adjusting design parameters to improve the thermal response of FinFETs, supporting the development of semiconductors and their applications in nanotechnology and advanced electronics. Such structures hold promise for biomedical applications, for example, in building portable systems for monitoring human biomedical parameters [15].

The FinFET transistor structure used for modeling the influence of channel length on the temperature dependence and I-V characteristics of the FinFET transistor with an optimal channel length of 20 nm is shown in Figure 8, a) and b) [16].

Conclusions

The conducted review shows that the next step in the development of three-dimensional GAA structures is the multilayer Forksheet and Nanosheet architectures. Thanks to the highly efficient gate-all-around (GAA) control of the FIN FET transistor channel and the small footprint on the chip, such structures can be successfully used for creating the elemental base of modern integrated circuits.

Additionally, the geometric dimensions of these three-dimensional GAA structures influence their thermal and current-voltage characteristics, opening up prospects for their use in sensor electronics, particularly in the development of magnetosensitive sensors, photosensitive sensors, and other types.

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Samarchuk O. – Leading Engineer of the Department of Computer Engineering and Electronics.

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Короткий порівняльний аналіз перспектив використання тривимірних FIN FET-транзисторів для сенсорної електроніки

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Розвиток сучасної електроніки грунтується на впровадженні сучасних мікро- та наноелектронних технологій. Традиційні комплементарні метал-оксид-напівпровідникові (КМОН) планарні транзисторні структури на основі масивного кремнію поступово поступаються більш досконалим структурам з кращими електричними, часовими, енергетичними характеристиками, радіаційною стійкістю на основі тривимірних структур (3D) «кремній-на-ізоляторі" які забезпечують кращі електричні характеристики, вищу швидкодію, енергоефективність з можливостями подальшого масштабування. Перспективними напрямами використання як для традиційних мікросхем, так і сенсорної електроніки є використання 3D-нанометрових транзисторів типу FinFET, Gate-All-Around (GAA), а також на основі нанолистів (Nano-sheet) та нанодротів (Nanowire). В роботі розглянуто структури таких типів КНІ нанометрових 3D-транзисторів і приклади можливостей їх використання у сенсорній електроніці.

Ключові слова: сенсорна електроніка, нанометрові структури «кремній-на-ізоляторі», кремнієві нанодроти, FinFET.