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The principle of developing a programmable multi-frequency oscillator based on CMOS transistors in the LT SPICE environment

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The paper examines the principle of operation of a ring oscillator and the method of its implementation on logic elements in order to improve its operation through simulation and an attempt to achieve optimal characteristics. Features of the implementation of a ring oscillator in the LT Spice environment using components such as a frequency divider, frequency generator, and frequency controller were also proposed.

The work investigated the operation of a frequency divider using five D-type flip-flops, from which six different frequencies were obtained (five flip-flops and one frequency at the generator output). Using LT Spice tools, time-frequency diagrams were constructed and the expected results were confirmed. The last step was to build a programmable oscillator and create a controller to set the desired frequency at the output of the device.

Keywords: CMOS transistor, ring oscillator, logic element, frequency controller, signal.

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Introduction

Currently, the rapid development of electronics and information technologies is causing the emergence of new tools for researching ring oscillators on CMOS transistors and methods for their development in software environments. Ring oscillators are devices for creating a signal of the desired shape, frequency, and amplitude.

The speed and reliability of the device will depend on the compliance of the signal characteristics with the requirements. All electronic devices depend on the correct operation of the generator, because it determines the rate of operation of the device. The paper will discuss the principle of operation of a ring oscillator and the method of its implementation, study of its operation through simulation and attempt to achieve optimal characteristics. The features of the implementation of a ring oscillator in the LTSpice environment using such components as a frequency divider, frequency generator and frequency encoder will be considered.

In general, the analysis of literary sources and the state of the problem showed the relevance of this topic and the need for further scientific and applied research to improve the design and development of ring oscillators based on CMOS transistors.

I. Ring generator on NOT logic elements.

To build a ring oscillator, you need series-connected inverters, which are available in the standard LT Spice library. A standard inverter has input voltage, output voltage, and control pins that can be used to change the inverter's operating mode depending on the voltage level applied to it[1]. By default, the operating mode input will be grounded.

Among the parameters for the inverter are logic high and low, V_{high} = 1 and V_{low} = 0 respectively, signal rise and fall times, T_{rise}=0 and T_{fal}l=T_{rise} respectively, output RC time constant Tau, output capacitance and impedance, C_{out} = 0 and Rout = 1 respectively.

Figure 1 shows the series-connected inverters from the LT Spice library implementing a ring oscillator. In this circuit, the inverter time delay parameter is set to 1 ns.

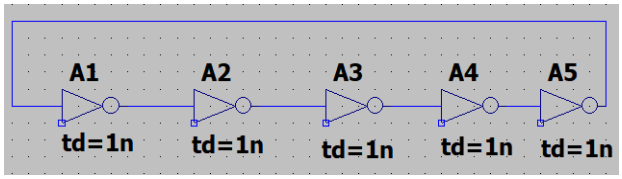

Fig. 1. Series-connected inverters in the LT Spice environment.

From the voltage-time diagram in Figure 2. we can determine the period of the signal generated by the inverters, which is 4ns. Hence, if the signal frequency is f.

$$f = \frac{1}{T} f = \frac{1}{T} \quad (1)$$

Then, substituting the value of the period, we get the frequency

$$f = \frac{1}{T} = \frac{1}{4ns} = \frac{1}{4 \cdot 10^{-9}} = 4 \cdot 10^{9} = 4GHz$$

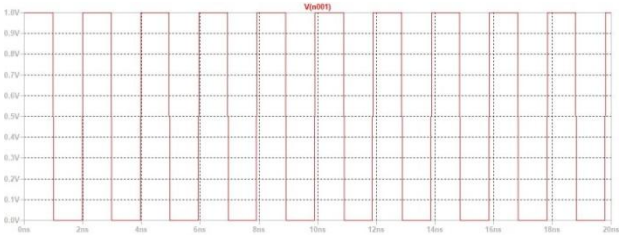

Fig. 2. Timing diagram of the ring oscillator signal.

Figure 3. shows the developed inverter based on p- and n-type MOS transistors, which is a CMOS transistor[2-3]. A constant voltage source with a nominal value of 1V is connected to the source and substrate of the p-type MOS transistor. The length parameter values of both transistors are 50nm.The gates of both transistors are connected to the IN pin for further connection in the circuit. The OUT pin is connected to the source of the p-type transistor and the drain of the n-type transistor.

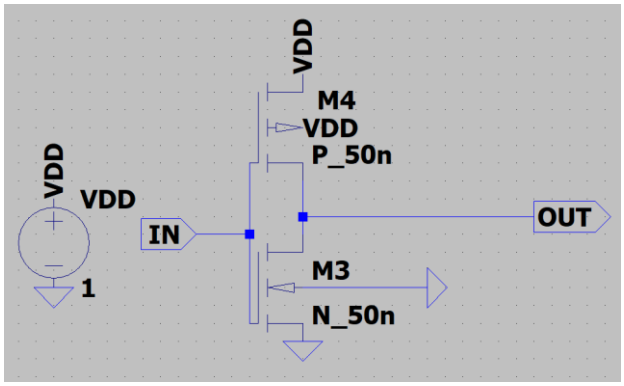

Fig. 3. CMOS inverter circuit diagram.

This inverter circuit can be represented using your own component, which will not differ functionally from the one above. Figure 4 shows the appearance of a component created based on this circuit.

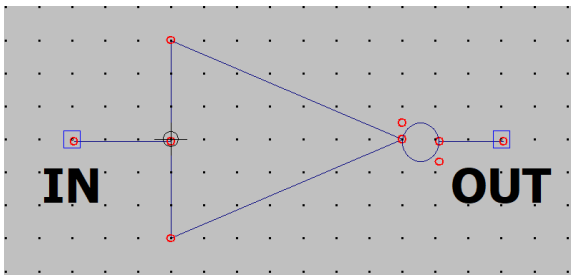

Fig. 4. Designed inverter based on CMOS transistor.

Figure 5 shows a diagram of series-connected inverters implementing a ring generator, but this time based on the developed inverter component.

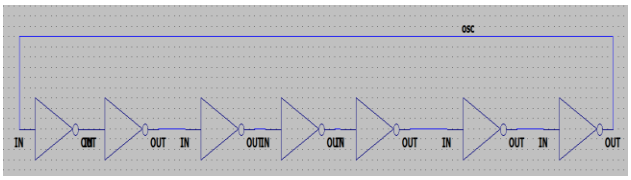

Fig. 5. Ring generator diagram.

Figure 6 shows a diagram of the dependence of voltage values on time, which shows the difference between a generator based on idealized inverters and inverters on a CMOS transistor with set physical parameters[4]. Now the generator signal more closely matches electrical processes in components. For example, the charge release that occurs after a capacitor is fully charged or discharged between different types of materials in transistors.

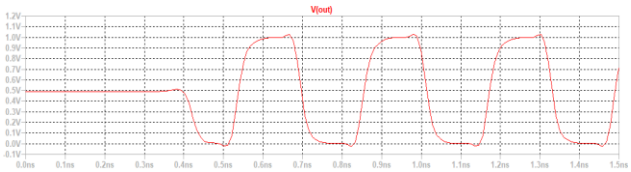

Fig. 6. Timing diagram of the signal at the generator output.

Based on this generator, we will create an OSCILLATOR component to abstract from the implementation for further use in other circuits. Figure 7 shows the appearance of the generator component with a single OUT output, which is the output of the maximum frequency signal. In the future, to change the maximum frequency, you need to change the number and parameters of inverters in the circuit.

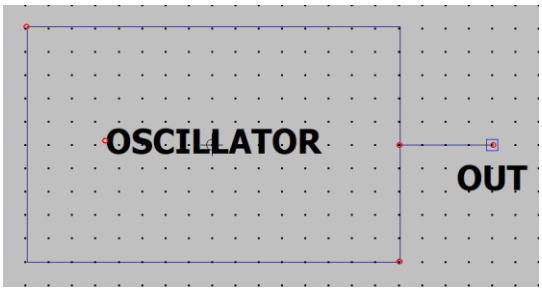

Fig. 7. Designed generator component.

II. Method of implementing a frequency divider.

Frequency is defined as the number of signal oscillations per unit of time, i.e. the main parameter for manipulating the frequency value will be time. In the construction of a ring oscillator, the main factor that allows changing a constant voltage value to a periodic alternating voltage is the time delay that occurs due to the switching characteristics of transistors. A similar principle can be used to construct a frequency divider[5].

The most well-known way to implement a frequency divider is with a series-connected D-type flip-flop, which is built on the basis of logic elements. The name of this type of flip-flop comes from the first letter of the English word delay, that is, delay, because the output value changes only when a repeated high voltage level is applied to its input (for positive logic). That is, when a periodic signal is input, for every two high voltage levels, there is one high voltage level at the output. In other words, the frequency of the trigger output signal is half the input frequency.

Since the output signal from the flip-flop is the same as the input signal, but modulated in frequency, it can be used as an input signal for another D-type flip-flop.[8-9] For example, if two flip-flops are connected in series, the input frequency fin will be applied to the first flip-flop, which will produce a signal with a frequency f1, which will be half the input frequency fin. After that, a signal with a frequency of f1 will be input to the second trigger, at the output of which a signal with a frequency of f1/2 or fin/4 will appear.

For easier calculations, let's take the input frequency equal to 2 to the power, for example, 10, which is equal to 1024, and construct a table of values of the function fout(n), where n is the number of D-type flip-flops connected in series.

Figure 8 shows a D-type flip-flop provided by LT Spice from the standard component library. The only input required for operation is the D input, to which the state setting signal is applied, the CLK input, to which the periodic control signal is applied, the Q output, from which the delay output state is taken, and the - Q output, which represents the inverted Q output[11].

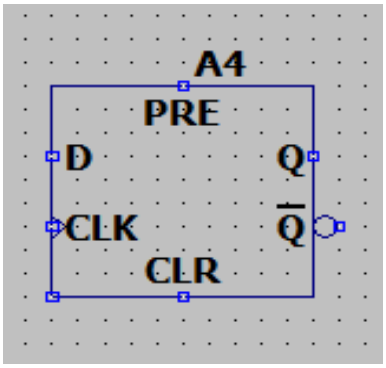

Fig. 8. D-type flip-flop from the LT Spice library.

The circuit diagram of the D-type series-connected flip-flops is shown in Figure 9. Among the possible methods of investigation, LT Spice provides the ability to analyze the transfer properties. In this scheme, the analysis takes place over 32ns, so that the output frequencies of the flip-flops are equal to 2 to some power [12]. Resistors R1-R4 are added to the circuit, because the environment allows you to measure the voltage drop across the elements. These resistances do not affect the time characteristics.

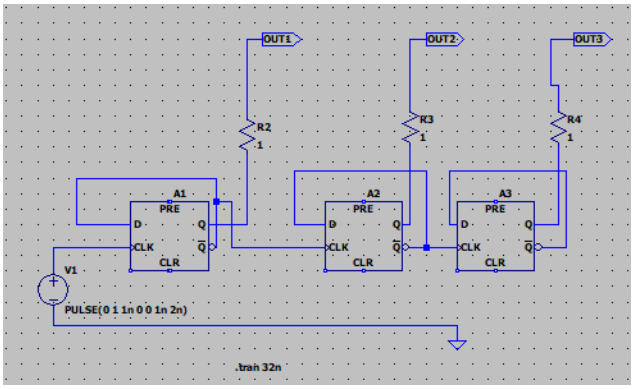

Fig. 9. Frequency divider.

Figures 10-13 show timing diagrams taken from the outputs of the triggers. The diagrams show how the signal frequency changes after passing through each trigger. It is worth noting that the diagrams are idealized for research where noise distortion is neglected.

Now that we have verified that the divider circuit works for the idealized signal, we can use the designed generator component. Figure 14 shows the circuit used above, but now the component we designed will be used as the signal generator.

The lower extremes of the signal are at a distance of .3354 ns, which is equal to the period of the signal. The frequency of this signal is 2.981GHz.

Figure 15. shows the time-frequency diagram of the signal. The input signal is marked in green, and the output signal from the first trigger is marked in blue. The diagram shows that the output signal of the trigger has half the period, or half the frequency.

Thus, a study of the operation of a frequency divider using five D-type flip-flops was conducted, from which six different frequencies were obtained (five flip-flops and one frequency at the generator output). Using LT Spice tools, we constructed frequency time diagrams and were able to verify the expected results. The final step in building a programmable oscillator will be to create a controller to set the desired frequency at the output of the device.

III. Frequency controller

The output frequency of a ring oscillator is the maximum possible frequency for it. For an arbitrary frequency value at the output of a ring oscillator, we will introduce the notation f_{max}. The frequency value will be largely determined by the parameters of the electrical components in the oscillator, such as the physical dimensions that affect capacitances and voltages, and the number of inverters. Achieving the maximum possible frequency value is not the task of the controller, as this is the responsibility of the manufacturers, who themselves implement the target requirements for the product. The

task of the controller will be to change the output frequency to that which will be determined by the input signals set by the user in a programmable way. Since the intermediate frequency value between the trigger contacts in the frequency divider is different, but deterministic, this can be used to output a signal with a certain frequency at the trigger output to the device output. Hence, we have the ability to change the output frequency by connecting the

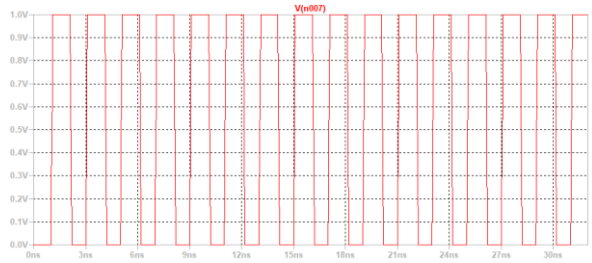

Fig. 10. Original signal.

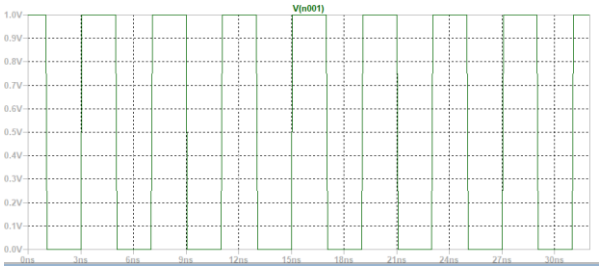

Fig. 11. Signal with frequency origina l/2

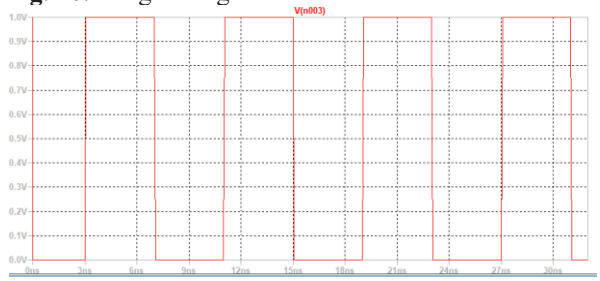

Fig. 12. Signal with frequency origina l/4

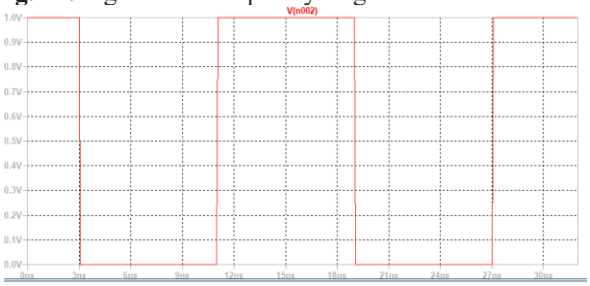

Fig. 13. Signal with frequency origina l/4

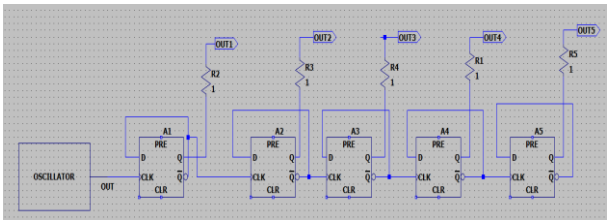

Fig. 14. Diagram of a signal frequency divider from a generator component.

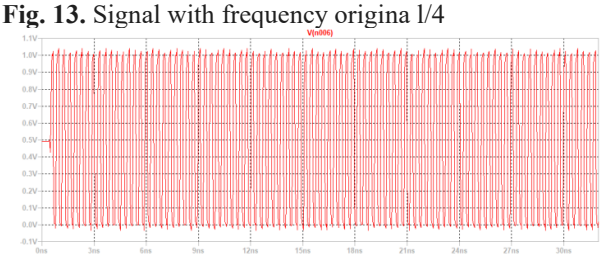

Fig. 15. Time diagram of the input signal frequency.

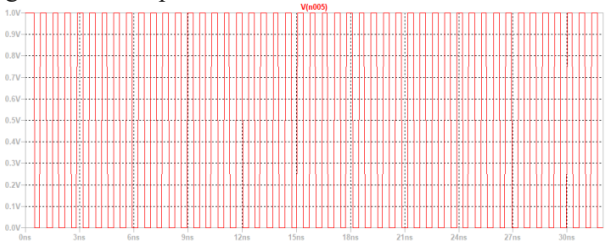

Fig. 16. Timing diagram of the first flip-flop with a frequency of 1.47GHz

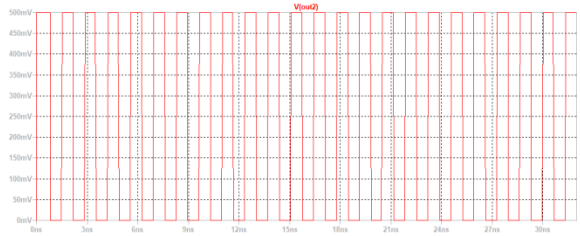

Fig. 17. Timing diagram of the second flip-flop with a frequency of 670 MHz

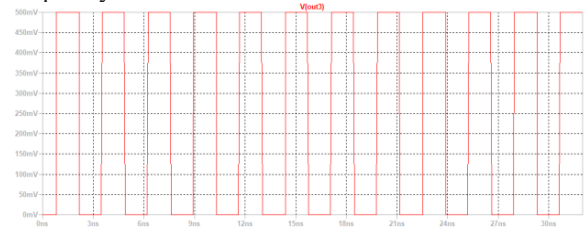

Fig. 18. Timing diagram of the second flip-flop with a frequency of 369 MHz

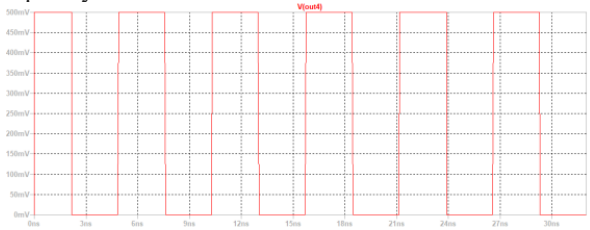

Fig. 19. Timing diagram of the second flip-flop with a frequency of 184 MHz

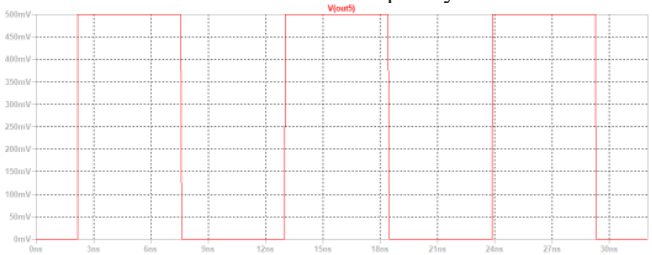

Fig. 20. Timing diagram of the second flip-flop with a frequency of 92 MHz.

generator output to the contact between the triggers. (Fig.21).

A common way to change the output signal would be to use transistor switches[13], controlled by a signal applied to the control pin. Since time is a key parameter, field effect transistors would be preferred, as bipolar transistors are used in most amplifiers where speed is not a key consideration. In addition, although the process of manufacturing an integrated circuit is not discussed in this work, it is worth noting that the use of MOS transistors will allow the technological process of creation to be combined into a single one.

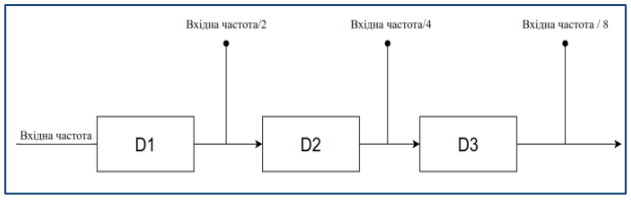

Fig. 21. Logic structure of a frequency divider based on D-type flip-flops.

Figure 22 shows an example of connecting the decoder to the pins connected from the D1-D4 flip-flops to the output. The input signal connected directly to the output is controlled by the decoder output Y0.

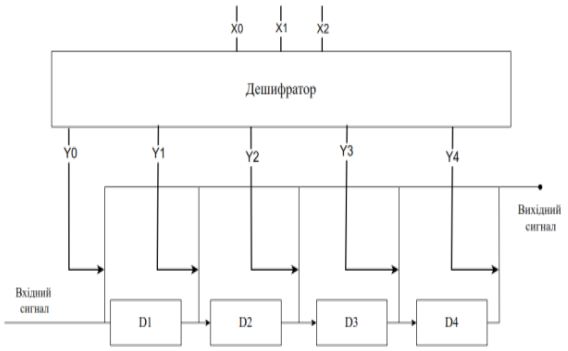

Fig. 22. Connecting the decoder to the outputs of the flip-flops in the frequency divider.

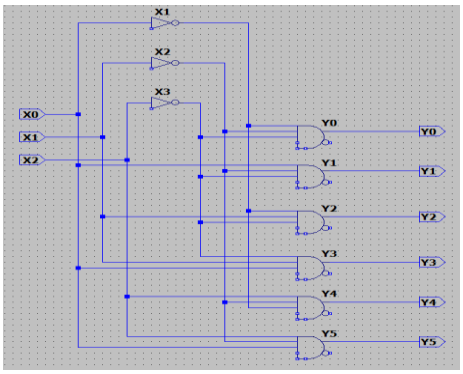

Fig. 23. 3-bit decoder with six outputs.

A 3-by-6 decoder component was developed using the LT Spice tool. Figure 24 shows the decoder symbol.

Since in this work the frequency divider will consist of 5 flip-flops, the decoder[14] must be 3-bit, because a 2-bit decoder can have a maximum of 4 outputs. In a 3-bit decoder, the number of outputs is 8, and the number of outputs from the frequency divider is 6 (5 flip-flops and one output of the initial frequency). The two extra outputs can simply be discarded.

Figure 23 shows the implemented circuit of a decoder with three inputs and six outputs.

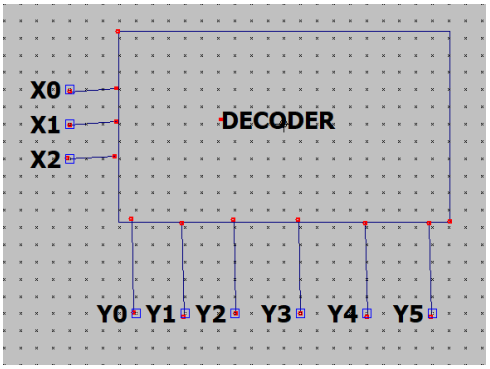

Fig. 24. Symbol of the developed decoder.

IV. Discussion of the results and prospects for the development of the method

The parameters of the width W and length L of the conduction channel are key for further calculations. The substrate and oxide layer of the transistor have the properties of a capacitor, in particular the charging and discharging time, which will determine the time and frequency values of the signal. The width value is common to the drain, source and gate.

It follows that the area of the gate will determine the charging and discharging times.

Increasing the width value increases the number of charge carriers, i.e., the current through the substrate.

Reducing the length of the channel, i.e. the conductor, also increases the current, but at a sufficiently small length, there is a risk of a short-channel effect, when the field strength under the gate increases due to a decrease in the distance between the drain and source, and accordingly, a decrease in the threshold voltage.

It was also investigated that with the given values for the n-type MONO transistor of length 50n and width 500n, and for the p-type parameters 50n and 1u, respectively, we obtain the frequency diagram shown in the figure. It can be seen that the signal fall and rise times are large enough to smooth the curve.

For the experiment, we tried to set the length of each transistor to twice as long. The figure shows a simulation diagram with new parameter values. It can be seen that when the transistor capacitance is charged, the voltage value increases rapidly, and a momentary discharge occurs. Then the voltage value remains at its maximum value until the voltage polarity changes. Until the desired behavior of the transistor charging is approached, it is necessary to try such a value of the parameter ratio that the duration of the trailing edge is minimal, even with a possible outage.

The next attempt was with the parameters of the p-type MOS transistor with a width of 60n and a length of 6u, and for the n-type 50n and 3u respectively. From the figure it is clear that the signal has the duration of the high and low signal levels closer to equal with a shorter fall

time and a relatively small increase in the duration of the step.

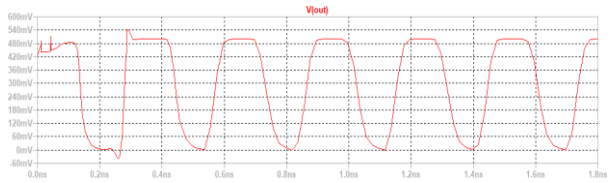

Fig 25. Signal diagram.

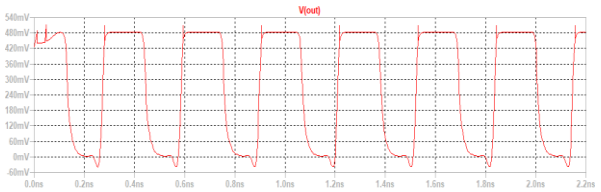

Fig. 26. Signal diagram.

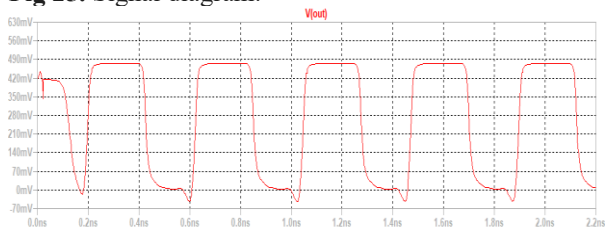

Fig. 27. Signal diagram.

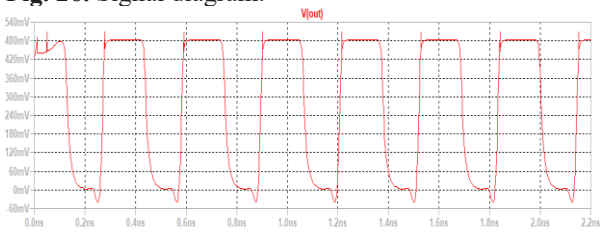

Fig. 28. Generator signal diagram with optimal parameters.

leading edge.

In addition, the signal frequency increased from .3ns to .4ns, which can be called a compromise when selecting transistor parameters.

Conclusions

This paper examines the principle of operation of a ring generator. It also discusses the main features of constructing this device in the LT Spice environment and the methods of research in it.

Using D-type flip-flops, a frequency divider method was implemented. This method allowed us to obtain frequency values that are multiples of the maximum output frequency. We will wait for new ways of implementing a frequency divider that will allow us to modulate a signal by frequency with a smaller division

A decoder was implemented to program the output frequency value, which made it possible to do without a complex system, i.e. the speed of the device's response to a change in the given frequency code remained optimal.

In this work, we were able to investigate the final circuit of a generator with programmable output frequency control based on a frequency divider. In addition, we examined the dependence of frequency on the physical dimensions of the transistors, from which we saw how critically these parameters affect the operation of the generator.

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Mamroha V.S. – fourth year student major 171 Electronics.

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Принцип розробленння програмованого багаточастотного генератора на КМОН транзисторах в середовищі LT SPICE

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В роботі розглянуто принцип роботи кільцевого генератора та спосіб його реалізації на логічних елементах з метою покращення його роботи за допомогою симуляції та спробі досягнути оптимальних характеристик. Також було запропоновано особливості реалізації кільцевого генератора у середовищі LTSpice за використання таких компонент як подільник частоти, генератор частоти та контролер частоти.

В роботі було проведено дослідження роботи подільника частоти з використанням п`яти тригерів D-типу, звідки було отримали шість різних частот (п`ять тригерів і одна частота на виході генератора). За допомогою інструментів LTSpice було здійснено побудову часових діаграм частот і змогли переконатись у очікуваних результатах. Останнім кроком була побудова програмованого генератора та створення контролера для задання бажаної частоти на виході пристрою.

Ключові слова: КМОН-транзистор, кільцевий генератор, логічний елемент, контролер частоти, сигнал.